Low-Voltage Op-amp Design and Simulation Using C5 500nm Process

Cody McDonald
EE420 Semester Project
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Design Specifications:

The goal of this design was to create an op-amp that using ON Semiconductor's C5 500nm process. The design would also need to operate with a minimum VDD of 2V while being able to drive a max 100pF and minimum 1K-Ohm loads. The additional parameters that needed to be fulfilled were the following:

- A DC open-loop gain greater than 66 dB under all load and VDD condition.
- A Gain-bandwidth product larger than 1 MHz
- A common mode rejection ratio (CMRR) greater than 90 dB at 100 kHz
- A power supply rejection ration greater than 90 dB at 100 kHz.
- A slew-rate with maximum load greater than 1V/microsecond.

MOSFET Characterization:

A vital aspect of this design is being able to correctly size the bodies of the transistors that we will be using in the start-up, beta-multiplier reference, diff-amp, and amplifier circuits.

The threshold voltage for the NMOS and PMOS will be determined graphically by plotting the drain current versus V_{GS} and V_{SG}.

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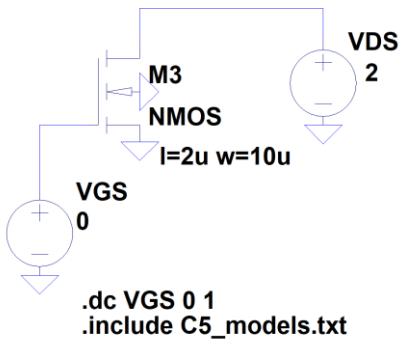
* BSIM3 models for AMI Semiconductor's C5 process
*
* Don't forget the .options scale=300nm if using drawn lengths
* and the MOSIS SUBM design rules
*
* 2<Ldrawn<500   10<Wdrawn<10000 Vdd=5V
* Note minimum L is 0.6 um while minimum W is 3 um
* Change to level=49 when using HSPICE or SmartSpice

.MODEL NMOS NMOS (                                LEVEL   = 8
+VERSION = 3.1           TNOM    = 27             TOX     = 1.39E-8
+XJ      = 1.5E-7        NCH     = 1.7E17         VTH0    = 0.6696061
+K1      = 0.8351612     K2      = -0.0839158     K3      = 23.1023856
+K3B     = -7.6841108    W0      = 1E-8           NLX     = 1E-9
+DVT0W   = 0             DVT1W   = 0              DVT2W   = 0
+DVT0    = 2.9047241     DVT1    = 0.4302695      DVT2    = -0.134857
+U0      = 458.439679    UA      = 1E-13          UB      = 1.485499E-18
+UC      = 1.629939E-11  VSAT    = 1.643993E5     A0      = 0.6103537
+AGS     = 0.1194608     B0      = 2.674756E-6    B1      = 5E-6
+KETA    = -2.640681E-3  A1      = 8.219585E-5    A2      = 0.3564792
+RDSW    = 1.387108E3    PRWG    = 0.0299916      PRWB    = 0.0363981
+WR      = 1             WINT    = 2.472348E-7    LINT    = 3.597605E-8
+XL      = 0             XW      = 0              DWG     = -1.287163E-8
+DWB     = 5.306586E-8   VOFF    = 0              NFACTOR = 0.8365585
+CIT     = 0             CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0             ETA0    = 0.024673B      ETAB    = -1.406123E-3
+DSUB    = 0.2543458     PCLM    = 2.5945188      PDIBLC1 = -0.4282336
+PDIBLC2 = 2.311743E-3   PDIBLCB = -0.0272914     DROUT   = 0.7283566
+PSCBE1  = 5.598623E8    PSCBE2  = 5.461645E-5    PVAG    = 0
+DELTA   = 0.01          RSH     = 81.8           MOBMOD  = 1
+PRT     = 8.621         UTE     = -1             KT1     = -0.2501
+KT1L    = -2.58E-9      KT2     = 0              UA1     = 5.4E-10
+UB1     = -4.8E-19      UC1     = -7.5E-11       AT      = 1E5
+WL      = 0             WLN     = 1              WW      = 0
+WWN     = 1             WWL     = 0              LL      = 0
+LLN     = 1             LW      = 0              LWN     = 1
+LWL     = 0             CAPMOD  = 2              XPART   = 0.5
+CGDO    = 2E-10         CGSO    = 2E-10          CGBO    = 1E-9
+CJ      = 4.197772E-4   PB      = 0.99           MJ      = 0.4515044
+CJSW    = 3.242724E-10  PBSW    = 0.1            MJSW    = 0.1153991
+CJSWG   = 1.64E-10      PBSWG   = 0.1            MJSWG   = 0.1153991
+CF      = 0             PVTH0   = 0.0585501      PRDSW   = 133.285505
+PK2     = -0.0299638    WKETA   = -0.0248758     LKETA   = 1.173187E-3
+AF      = 1             KF      = 0)
*
.MODEL PMOS PMOS (                                LEVEL   = 8
+VERSION = 3.1           TNOM    = 27             TOX     = 1.39E-8
+XJ      = 1.5E-7        NCH     = 1.7E17         VTH0    = -0.9214347
+K1      = 0.5553722     K2      = 8.763328E-3    K3      = 6.3063558
+K3B     = -0.6487362    W0      = 1.280703E-8    NLX     = 2.593997E-8
+DVT0W   = 0             DVT1W   = 0              DVT2W   = 0
+DVT0    = 2.5131165     DVT1    = 0.5480536      DVT2    = -0.1186489
+U0      = 212.0166131   UA      = 2.807115E-9    UB      = 1E-21
+UC      = -5.82128E-11  VSAT    = 1.713601E5     A0      = 0.8430019
+AGS     = 0.1328608     B0      = 7.117912E-7    B1      = 5E-6
+KETA    = -3.674859E-3  A1      = 4.77502E-5     A2      = 0.3
+RDSW    = 2.837206E3    PRWG    = -0.0363908     PRWB    = -1.016722E-5
+WR      = 1             WINT    = 2.838038E-7    LINT    = 5.528807E-8
+XL      = 0             XW      = 0              DWG     = -1.606385E-8
+DWB     = 2.266386E-8   VOFF    = -0.0558512     NFACTOR = 0.9342488
+CIT     = 0             CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0             ETA0    = 0.3251882      ETAB    = -0.0580325
+DSUB    = 1             PCLM    = 2.2409567      PDIBLC1 = 0.0411445
+PDIBLC2 = 3.355575E-3   PDIBLCB = -0.0551797     DROUT   = 0.2036901
+PSCBE1  = 6.44809E9     PSCBE2  = 6.300848E-10   PVAG    = 0
+DELTA   = 0.01          RSH     = 101.6          MOBMOD  = 1
+PRT     = 59.494        UTE     = -1             KT1     = -0.2942
+KT1L    = 1.68E-9       KT2     = 0              UA1     = 4.5E-9
+UB1     = -6.3E-18      UC1     = -1E-10         AT      = 1E3
+WL      = 0             WLN     = 1              WW      = 0
+WWN     = 1             WWL     = 0              LL      = 0
+LLN     = 1             LW      = 0              LWN     = 1
+LWL     = 0             CAPMOD  = 2              XPART   = 0.5
+CGDO    = 2.9E-10       CGSO    = 2.9E-10        CGBO    = 1E-9
+CJ      = 7.235528E-4   PB      = 0.9527355      MJ      = 0.4955293
+CJSW    = 2.692786E-10  PBSW    = 0.99           MJSW    = 0.2958392
+CJSWG   = 6.4E-11       PBSWG   = 0.99           MJSWG   = 0.2958392
+CF      = 0             PVTH0   = 5.98016E-3     PRDSW   = 14.8598424
+PK2     = 3.73981E-3    WKETA   = 5.292165E-3    LKETA   = -4.205905E-3
+AF      = 1             KF      = 0)
```

Figure 1:LTSpice model providing the MOSFET parameters for the op-amp



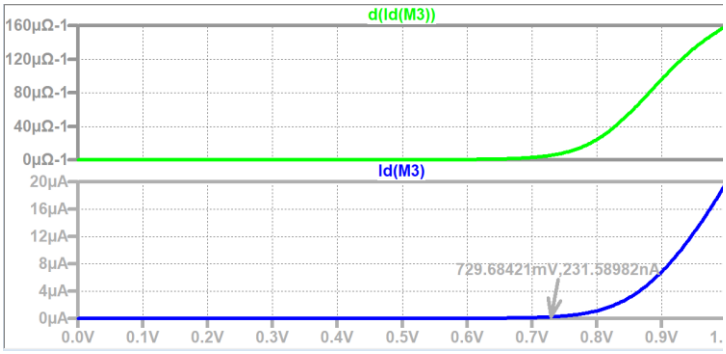
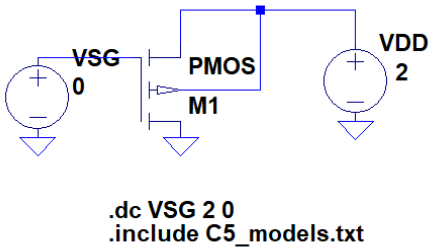


Figure 2: NMOS characterization - V_{GS} vs I_D

Sweeping V_{GS} from 0 to 1V reveals the threshold voltage to be approximately 0.73V. The derivative of the drain current is taken in the top plot plane to more easily see when the current begins to increase.



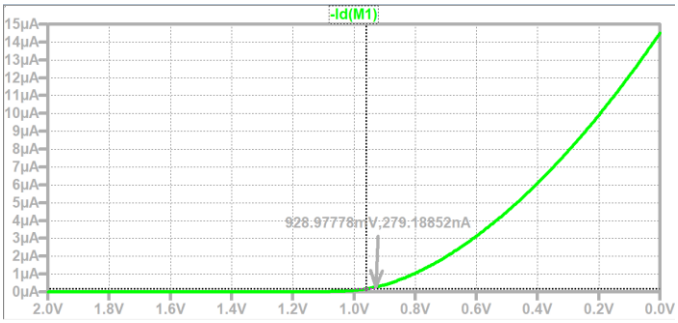


Figure 3: PMOS Characterization - V_{SG} vs I_D

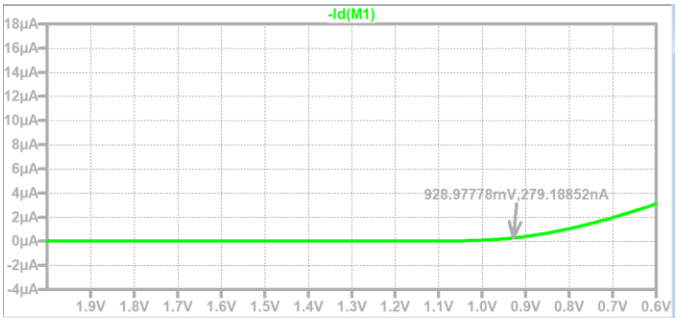


Figure 4: Zoomed view of Figure 2

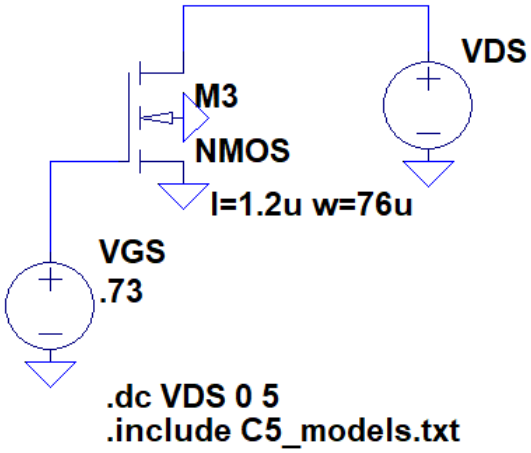
The PMOS was observed to have a threshold voltage of 0.93V.

The next parameter to be found is the bias current. A low bias current will allow for a smaller overdrive voltage, which is necessary for a more resilient design.

Choosing Bias Current:

To choose the bias current I swept VDS and VSD vs VGS and determined the current at a VDD of 2V (the minimum operation voltage).

I chose a bias current of 8.5uA since a higher bias current would have resulted in a higher PMOS width length. I stopped around 8.5uA since the PMOS width appeared to be getting too large.



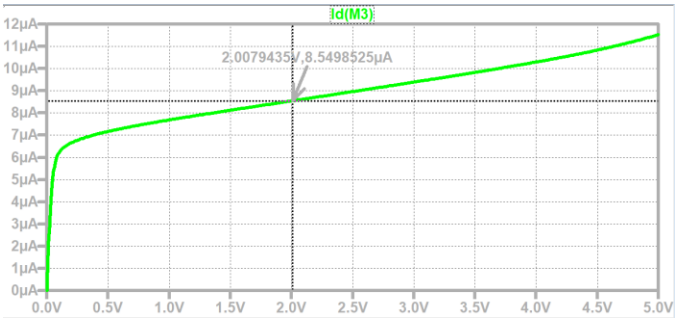
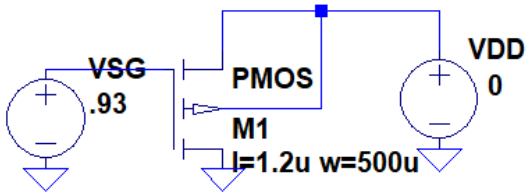


Figure 5:ID vs VDD for NMOA



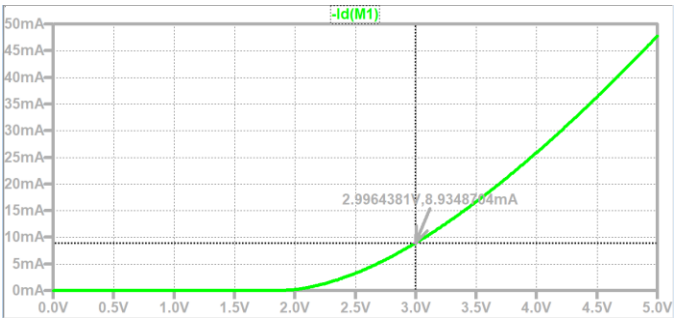


Figure 6:ID vs VDD for PMOS

Summarized Table:

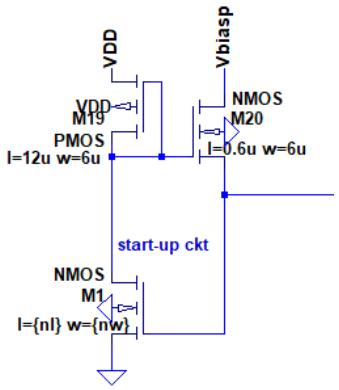
Characteristics	*NMOS*	*PMOS*
Bias Current I_D	*8.5uA*	*8.5uA*
W/L	*76/1.2*	*500/1.2*
W/L (Actual)	*40/0.6*	*90/0.6*
$V_{DS,Sat}$ and $V_{SD,Sat}$	*55mV*	*55mV*
V_{GS} and V_{SG}	*785mV*	*875mV*
V_{THN} and V_{THP}	*730mV*	*930mV*
K_{Pn} and K_{Pp}	*332uA/v^2*	*44.4uA/v^2*
Cox'	*2.4831 fF/um^2*	*2.4831 fF/um^2*
Cox_n and Cox_p	*85.82fF*	*644fF*
Cgs_n and Csg_p	*31.6fF*	*25.9fF*
Cgd_n and Cdg_p	*7.9fF*	*25.9fF*
gm_n and gm_p	*227uA/V*	*228uA/V*
lambda	*0.25 v^{-1}*	*0.138v^{-1}*

Table 1:MOSFET Characterization obtained from LTSpice error list of BMR Circuit

Building the Reference Circuit:

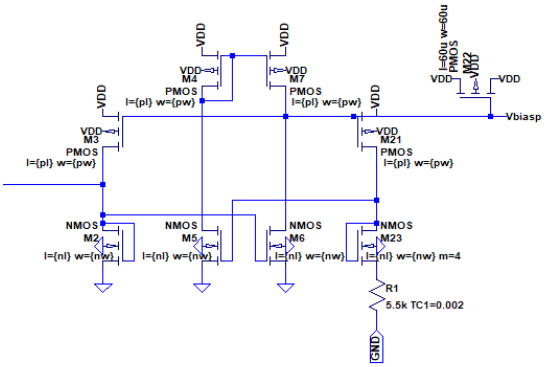
This device requires a biasing circuit to provide voltages references for the actual op-amp. The primary focus of this circuit is to ensure that the voltages and currents won't vary with changes in the power supply voltage (VDD). Alone a BMR circuit would be subject to this operation, however adding a diff-amp to the circuit would fix this problem.

Start-up circuit:



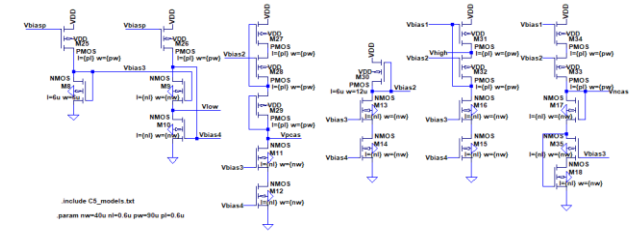
The startup circuit prevents the self-biased circuit from going into cut-off mode. Should the circuit turnoff, the circuit would have zero current flowing through it and render the design useless.

Diff-amp + BMR:



As previously stated, the Diff-amp/BMR combo prevents the current and voltage changes as a result of changes in VDD, however this design can cause instability throughout the rest of the circuit. The transistor, M22, is used to compensate for this effect.

Bias Circuit:



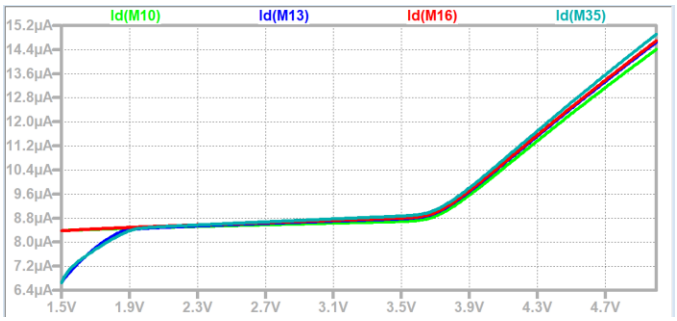


Figure 7:Bias currents through each of the branches

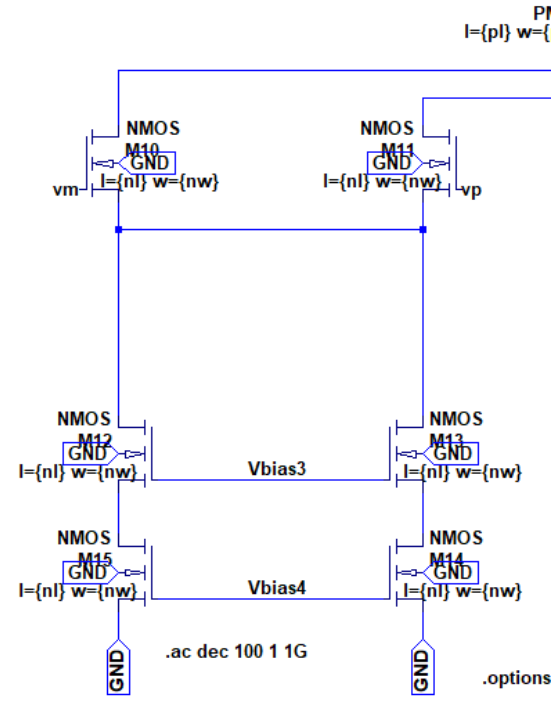
Sweeping VDD from 1.5V to 5V shows a stable current of 8.7uA from 1.5V to 3.7V. I assumed there would be instability in my circuit after I crossed 3.7V, however the op-amp appeared to operate normally.

Amplifier Design:

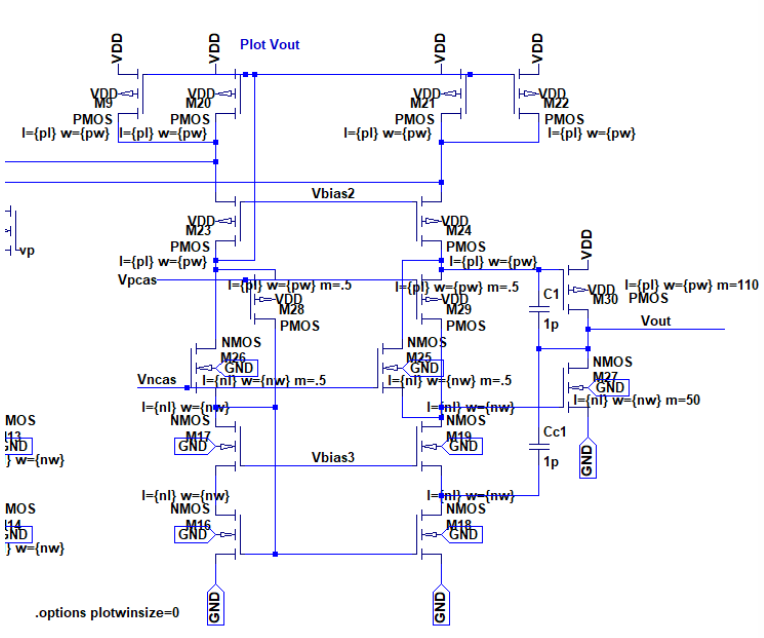
The amplification design of this device will utilize another Diff-Amp in conjunction with a Push-Pull amplifier.

I originally selected my body sizes based on general design choices by selecting a length to be twice the times of the minimum length and choosing a width similar to body sizes calculated in Table 1. I would later change the length to the minimum length in order to obtain quicker speed. These body sizes would then be manipulated to achieve the desired specifications of the project.

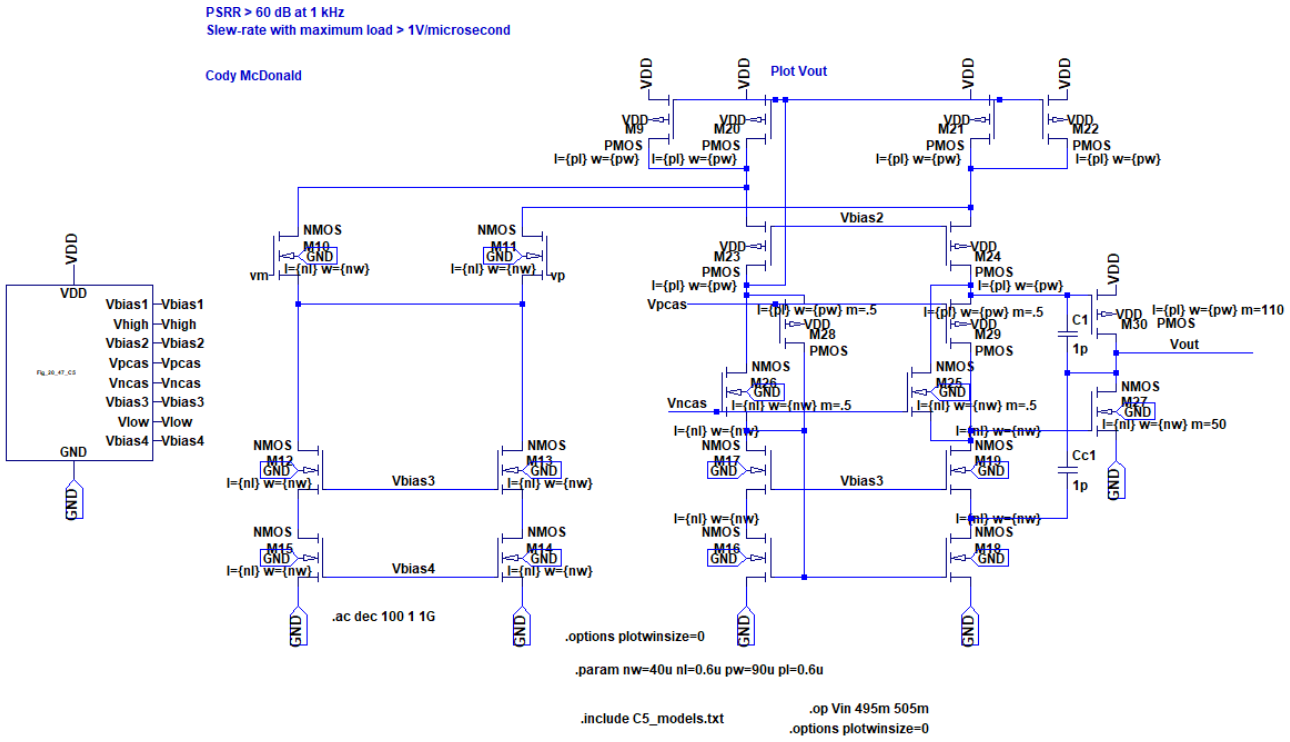
Diff-Amp:



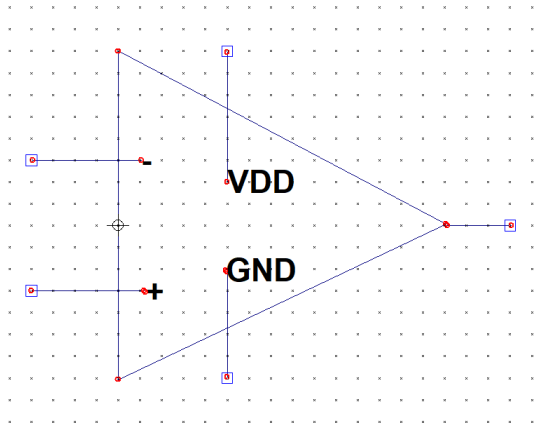
Push-pull:



Full Circuit:



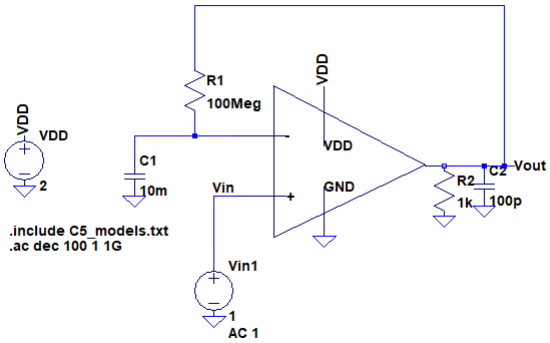
Op-Amp Symbol for Circuit:



The is the symbol I used to represent the full circuit above including the bias circuit.

Op-Amp Performance:

DC Open Loop Gain:



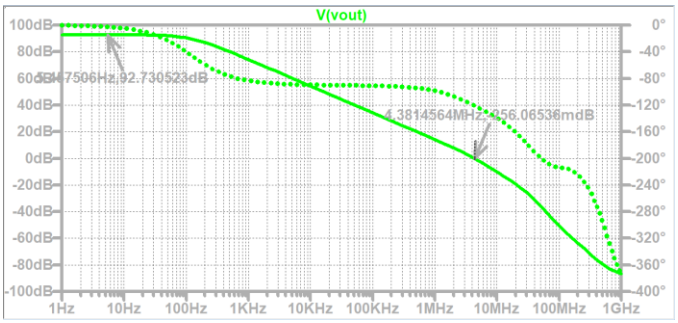


Figure 8:DC Open Loop Gain Under load conditions

With a full capacitive and resistive load, the DC open loop gain of this device is 92dB with a unity gain frequency of 4.3MHz, which satisfies the requirement of the gain bandwidth product over 1MHz.

The gain bandwidth product could also be calculated using the following pole splitting method:

$$f_{un} = \frac{g_{m1}}{C_c}$$

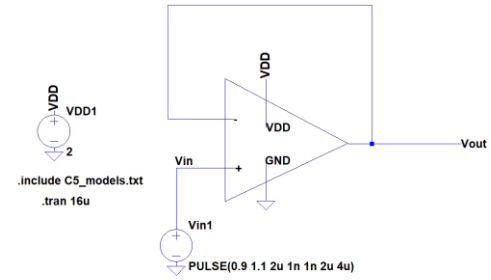
To calculate g_{m1} we must calculate the sums of the transconductances.

$$g_{m1} = g_{mn} + g_{mp} = 227\frac{\mu A}{v} + 228\frac{\mu A}{v} = 455\frac{\mu A}{v}$$

Substituting this back into the unity frequency equation I get:

$$f_{un} = 4.55MHz$$

Step Response:



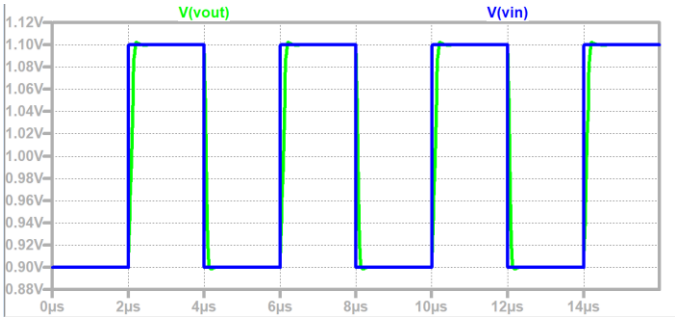
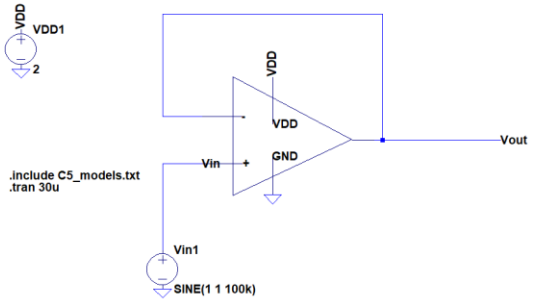


Figure 9: Step Response

The step response is a great indicator of the stability of the device and how it will operate given an input signal. This was tested by inputting a pulsed wave to resemble a step response into the op-amp. A high amount of overshoot means the device is rather unstable. I was able to correct this by decreasing the gain of the device. This was greatly influenced by adjusting the width multipliers in transistors M27 and M30.

Output Swing:



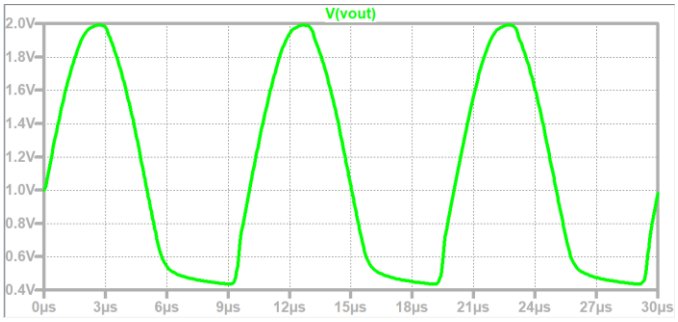
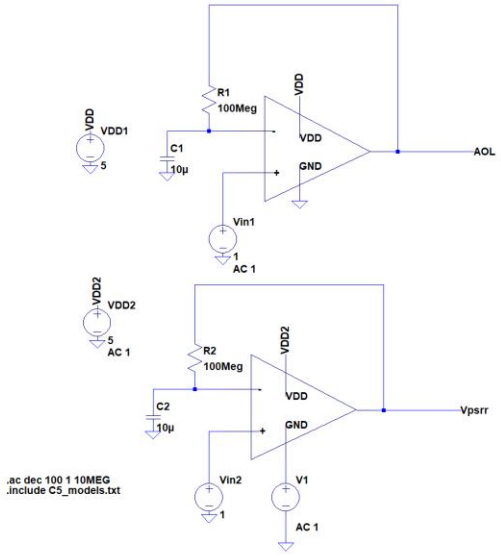


Figure 10: Output Swing

The output swing of the device extended from 0.42V to 2V. The upward swing of the output extended to 2V, which was the goal however the down swing of the signal didn't fully approach 0V.

Power Supply Rejection Ratio (PSRR):



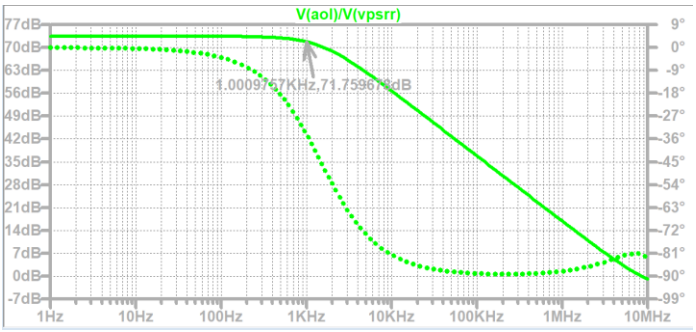
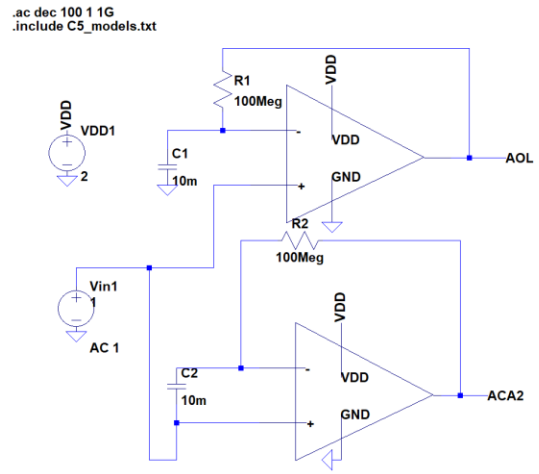


Figure 11:PSSR

The power supply rejection ratio comfortably fits within the design parameters as it measures out at 71.2dB at a frequency of 1KHz, which fits into the specification of 60dB at 1KHz. The PSRR was also tested at a VDD of 2v where I obtained a PSRR of 66.0dB

Common Mode Rejection Ratio:



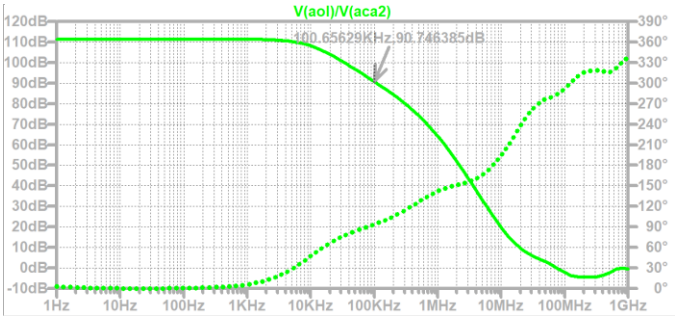


Figure 12: CMRR

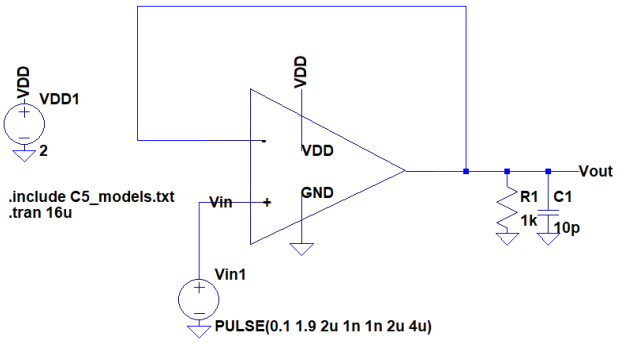
The CMRR of the device was able to meet specification of this design as the frequency response shows 90.7dB at 100KHz.

The CMRR can be calculated from the equation

$$CMRR = 20\log(\frac{A_{OL}(f)}{Ac*A_2})$$

Therefore, the CMRR can be increased by increasing the open-loop gain. This would become a challenge as I would have to choose between increasing gain in exchange for decreased device speed, which would affect the slew-rate.

Slew Rate:



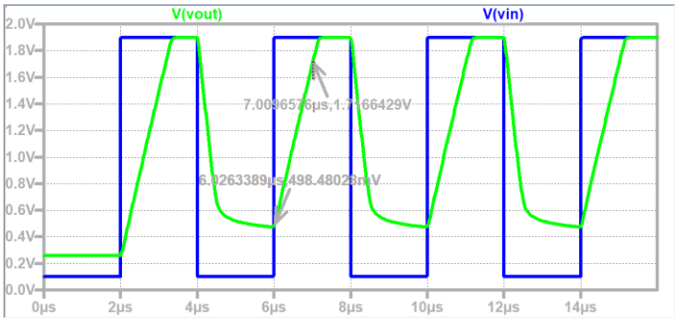


Figure 13:Slew Rate

The slew-rate is a good indicator of how quickly our device operates or responds to an input. Here I was able to calculate the slew-rate to be $1.71V - 498mV \rightarrow 1.282\frac{V}{\mu S}$, which completes the requirement of a slew-rate being at 1V per microsecond. This parameter was slightly challenging as I needed to sacrifice gain in exchange for higher speed. However, after testing many different parameters, I found that changing the overall lengths of the MOSFETS to 0.6um greatly increased the speed.

Input CMR As A function of V_{DD}

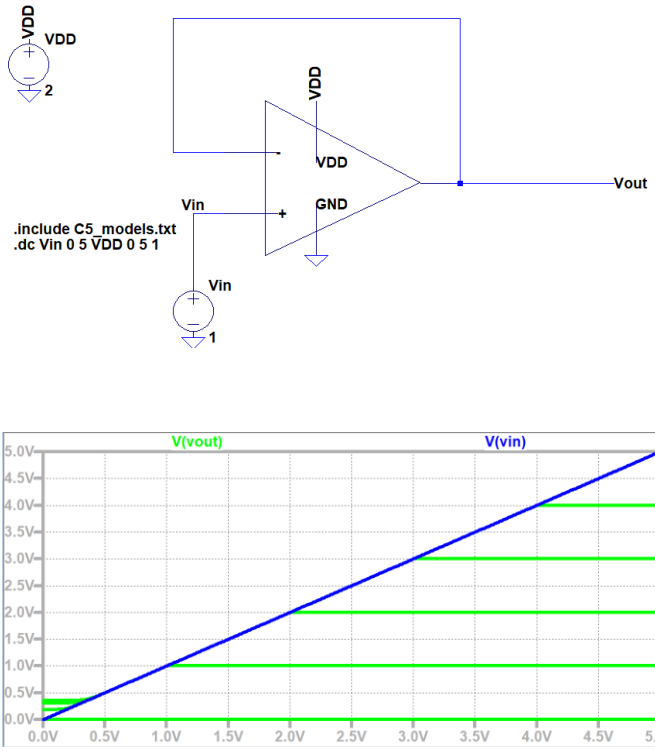
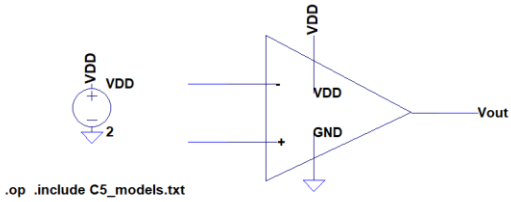


Figure 14: Vout vs incrementing VDD

Power Consumption:




```
* C:\Users\Cody\Documents\UNLV\Spring2019\EE420\lecture projec...
        --- Operating Point ---

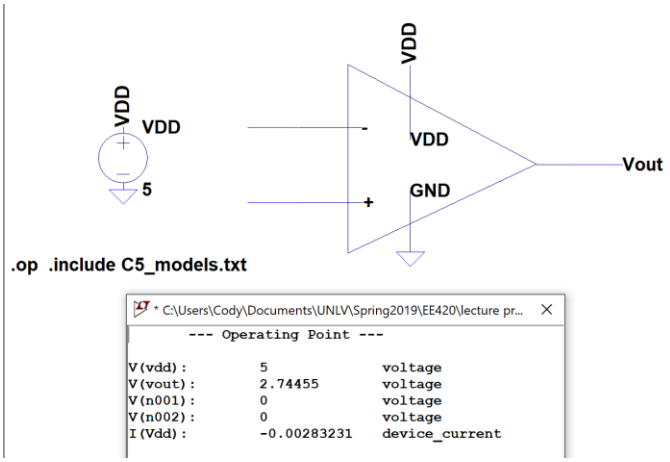
V(vdd):         2               voltage
V(vout):        1.11159         voltage
V(n001):        0               voltage
V(n002):        0               voltage
I(Vdd):         -0.000627072    device_current
```

The quiescent current draw of the device is 0.62mA, so the power consumption would be:

$$Power = 0.62mA * 2v = 1.24mW$$

The overall power consumption would be 1.24mW

At a higher VDD of 5V I obtained the following:



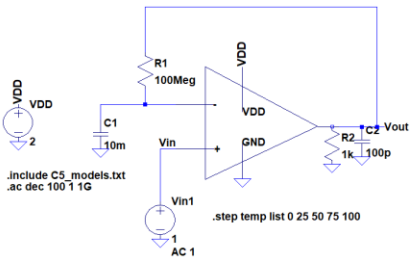

```
* C:\Users\Cody\Documents\UNLV\Spring2019\EE420\lecture pr...
        --- Operating Point ---

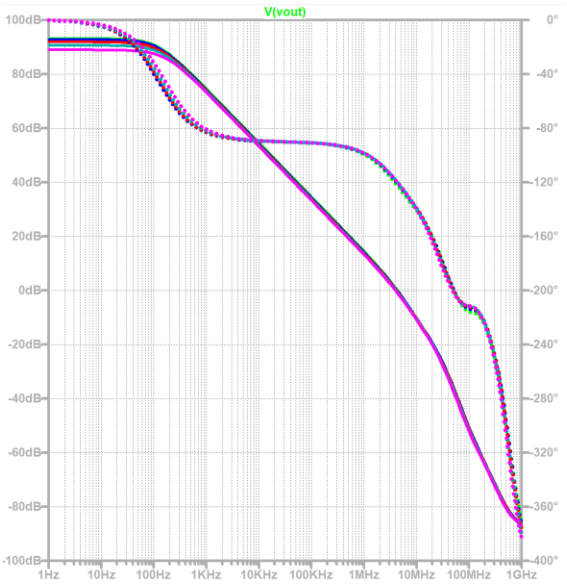
V(vdd):         5               voltage
V(vout):        2.74455         voltage
V(n001):        0               voltage
V(n002):        0               voltage
I(Vdd):         -0.00283231     device_current
```

The current draw at this VDD was 2.83mA, so the quiescent power consumption would be

$$Power = 2.83mA * 5v = 6.2mW$$

Temperature Testing:





This device's gain decreases with increases in temperature.

Summarized Data Table:

Specifications	2v	5v
Open-Loop Gain	92.6dB	90.4dB
Gain Bandwidth Product	4.38MHz	7.68MHz
Slew-Rate	1.282 v/uS	4.28v/uS
CMRR at 100KHz	90.7dB	84.3dB
PSRR at 1KHz	66.0dB	71.2dB
Quiescent Power Consumption	1.24mW	6.2mW

Output Swing	0.42v to 2v
VDD Operating Range	2v to 5v
Input CMR	-785mV to VDD + 685mV