Cody McDonald

EE 421 Digital IC Design

R. Jacob Baker

Boost Switching Power Supply Design

Introduction:

A Boost Switching Power Supply (SPS) is a device that boosts the power supply voltage of a device to a voltage that is higher than the input VDD. For example, using the design parameter goal for this design being a VDD = 3.75V to 5.25V, the Boost SPS will boost the output voltage to a constant 7.5V, which is the other design parameter goal for this project.

Design Parameters:

The project goal is to create a CMOS Boost SPS with a VDD that can vary from 3.75 to 5.25 V. The power supply will also require the use of off–chip components: Schottky diode, inductor, and capacitor to generate a constant output voltage of 7.5 V. The design must be able to handle load currents from 0 to 20 mA.

Design Note:

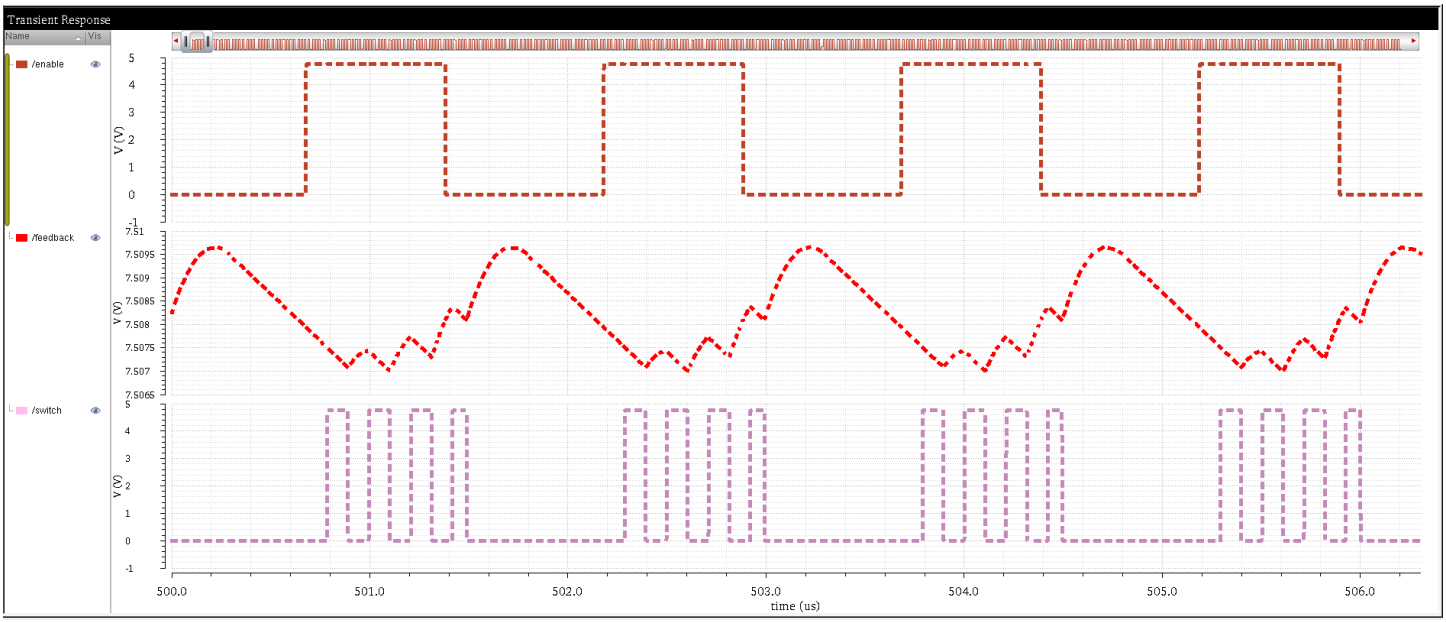
All layouts, schematics, and simulations were ran using Cadence. All schematics and layouts were tested and verified using DRC and LVS.

Overview: Boost SPS

The Boost SPS works via a collection on-chip and off-chip components. The components located onboard the chip are the oscillator, comparator, bandgap voltage reference circuit, the voltage feedback voltage divider, and the transistor switch. The off-chip components include a Schottky-diode, load-capacitor, resistive load, and inductive driver.

The enable signal from the comparator will be set to high if the feedback/output voltage shows to be less than 7.5V. This will then trigger the oscillator to oscillate. If the reverse case occurs, the enable signal will be set low if the voltage is higher than 7.5V and the oscillator will remain off. This system can be seen in the following simulation:

Boost SPS Operation with VDD = 4.75V



As the feedback voltage is approaching < 7.5V the enable will signal on and cause the oscillator to begin oscillating, which in turn bumps the voltage back up. Once the comparator notices the voltage is above 7.5V the enable will go low and cause the oscillator to shut-off. The output voltage will then begin to go down.

It must also be noted that the fluctuation in output voltage is the ripple voltage. In the above test case with VDD = 4.75V the ripple voltage is approximately 2mV, which is fairly stable.

Summary:

Feedback Current at Varying VDD	
VDD	Feedback I(AVG) (uA)
3.75	35.2
4.125	36.75
4.5	36.78
4.875	36.82
5.25	36.82

Output Voltage at Varying Temperatures	
Temperature (Celsius)	Output Voltage (Volts)
0	7.514
25	7.509
50	7.499
75	7.485

Efficiency at Varying VDD		
VDD	Source current draw (A)	Efficiency
3.75	0.03921	1.020147921
4	0.04028	0.930983118
4.25	0.03819	0.924171711
4.5	0.03635	0.917010546
4.75	0.03459	0.912950199
5	0.03316	0.904704463
5.25	0.03055	0.935234978

Output Voltage Vs. VDD	
VDD (V)	Output Voltage (V)
3.75	7.45
3.91	7.49
4.08	7.495
4.25	7.499
4.41	7.502
4.58	7.505
4.75	7.509
4.91	7.511
5.08	7.5165
5.25	7.55

Part 1: Bandgap Voltage Reference Circuit

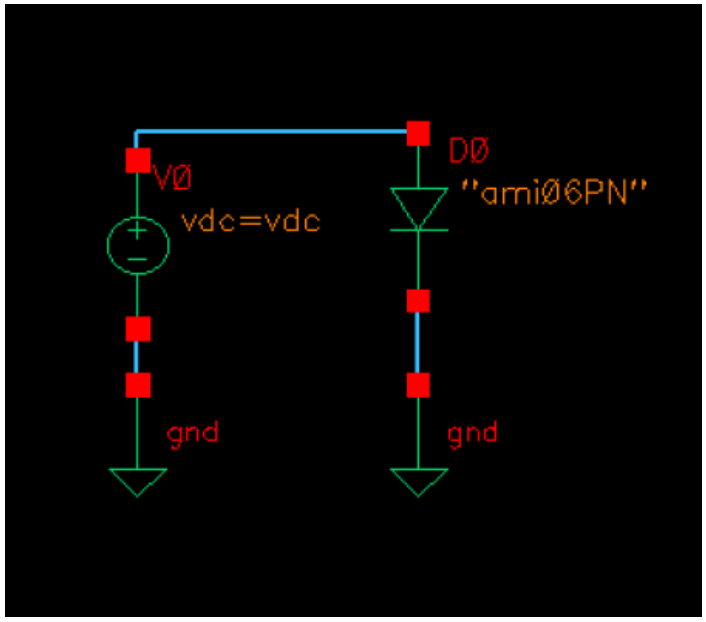
The bandgap voltage reference circuit is a circuit that will output a constant specified voltage regardless the input VDD. The topology of the circuit used in this design is also resilient towards changes in temperature and will be able to withstand the VDD range for this project of 3.75V to 5.25V.

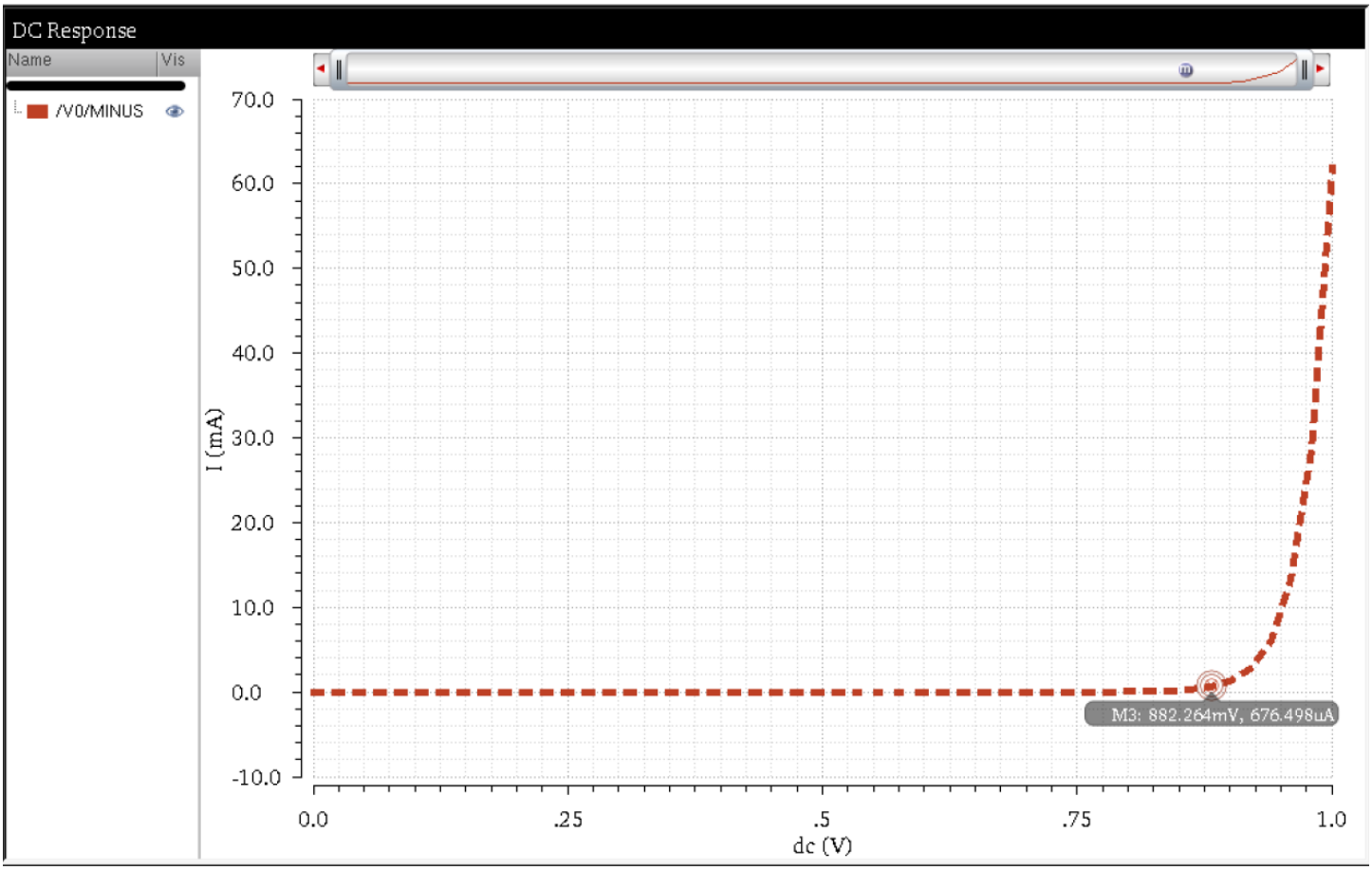
The Boost SPS will compare a feedback voltage with the reference voltage generated by the bandgap circuit. The voltage reference for this design will be Vref = 1.25V. This value is fed into a comparator, which will dictate whether the feedback voltage has fallen below or exceeded the reference voltage.

The bandgap reference device is an important component in this design as it is the reference point for the comparator to compare the output voltage too. Testing for this device must be conducted to determine how much of a variation can occur between changes in VDD and temperature change.

First, the parasitic diode in the bandgap circuit will be tested:

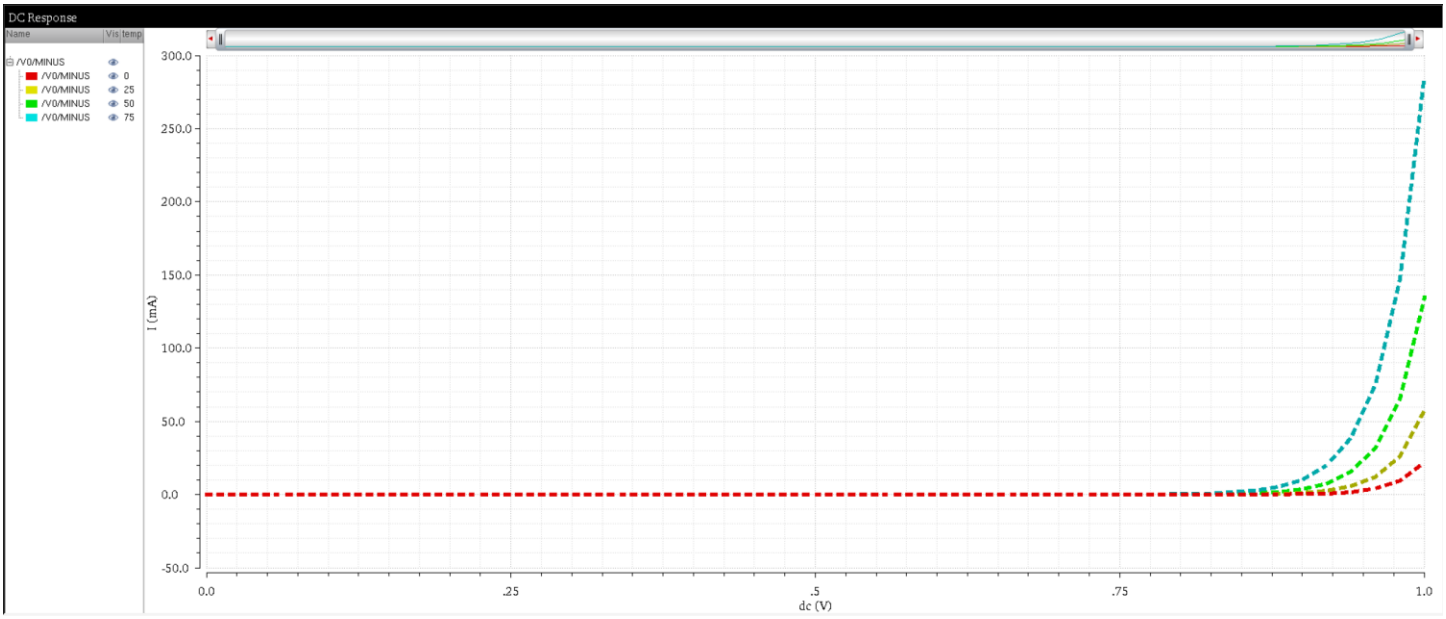
Parasitic Diode Testing:





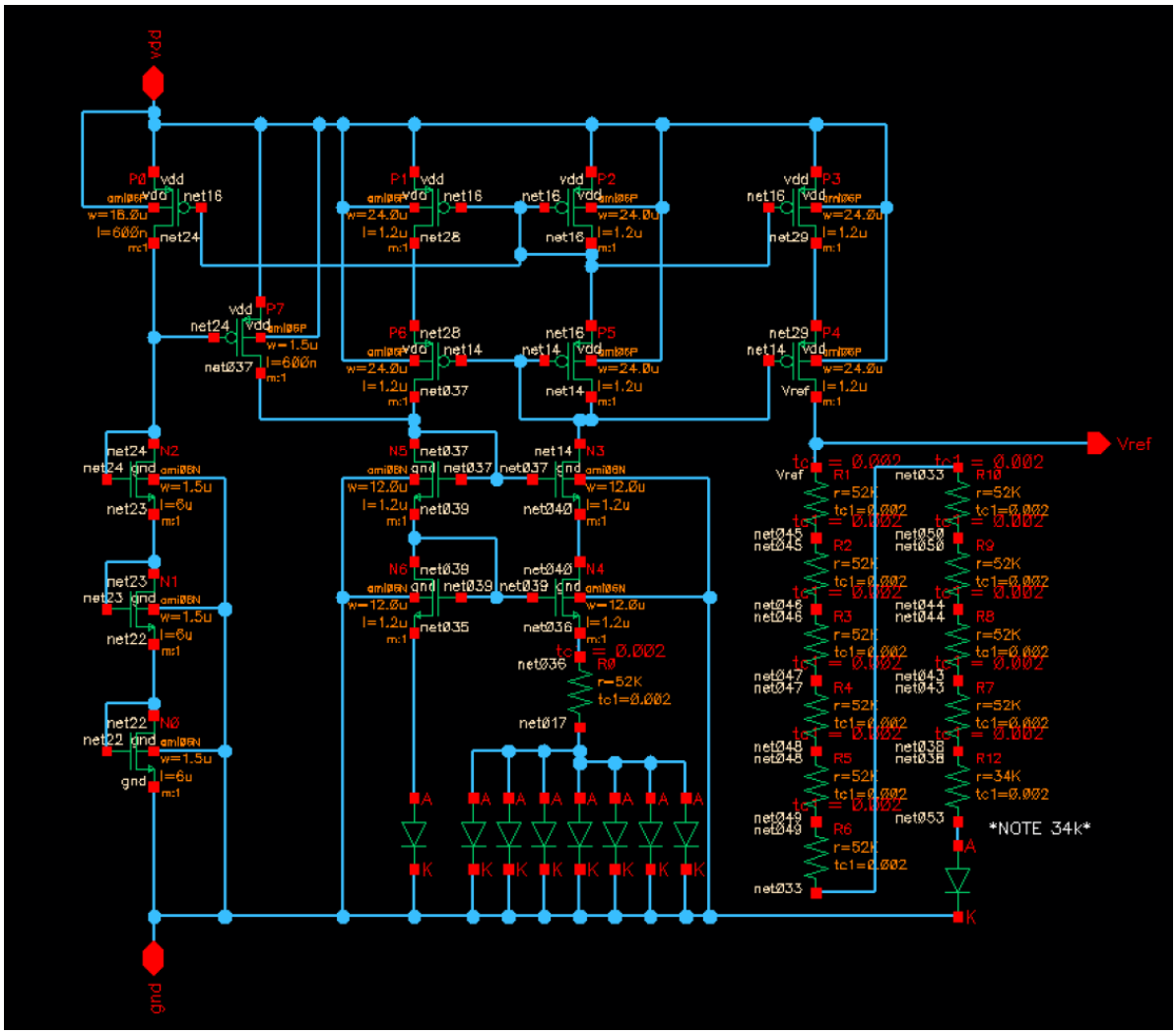
Given the simulation, the pnp parasitic-diode is roughly 900mV which is bit higher than the typical number for the built-in potential for diodes of this type. Despite the higher breakthrough voltage, the diode will still be useable for this design. This means the voltage potential before the device must reach 900mV before the device begins to pass current.

Parasitic Diode Potential Vs. Temperature:



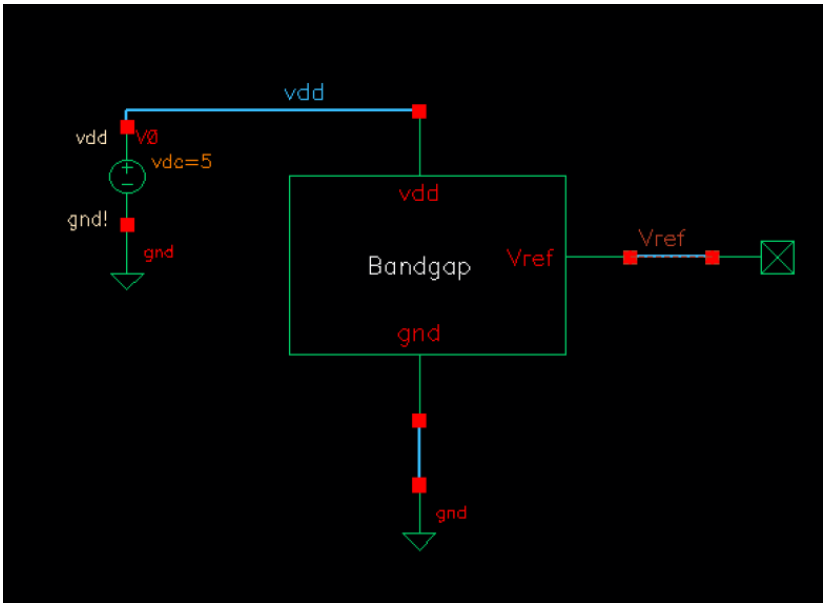
The parasitic diode potential moves further back as temperature increases. It is fair to assume that the overall performance of the bandgap will change as the design is also reliant on the operation of the parasitic diode.

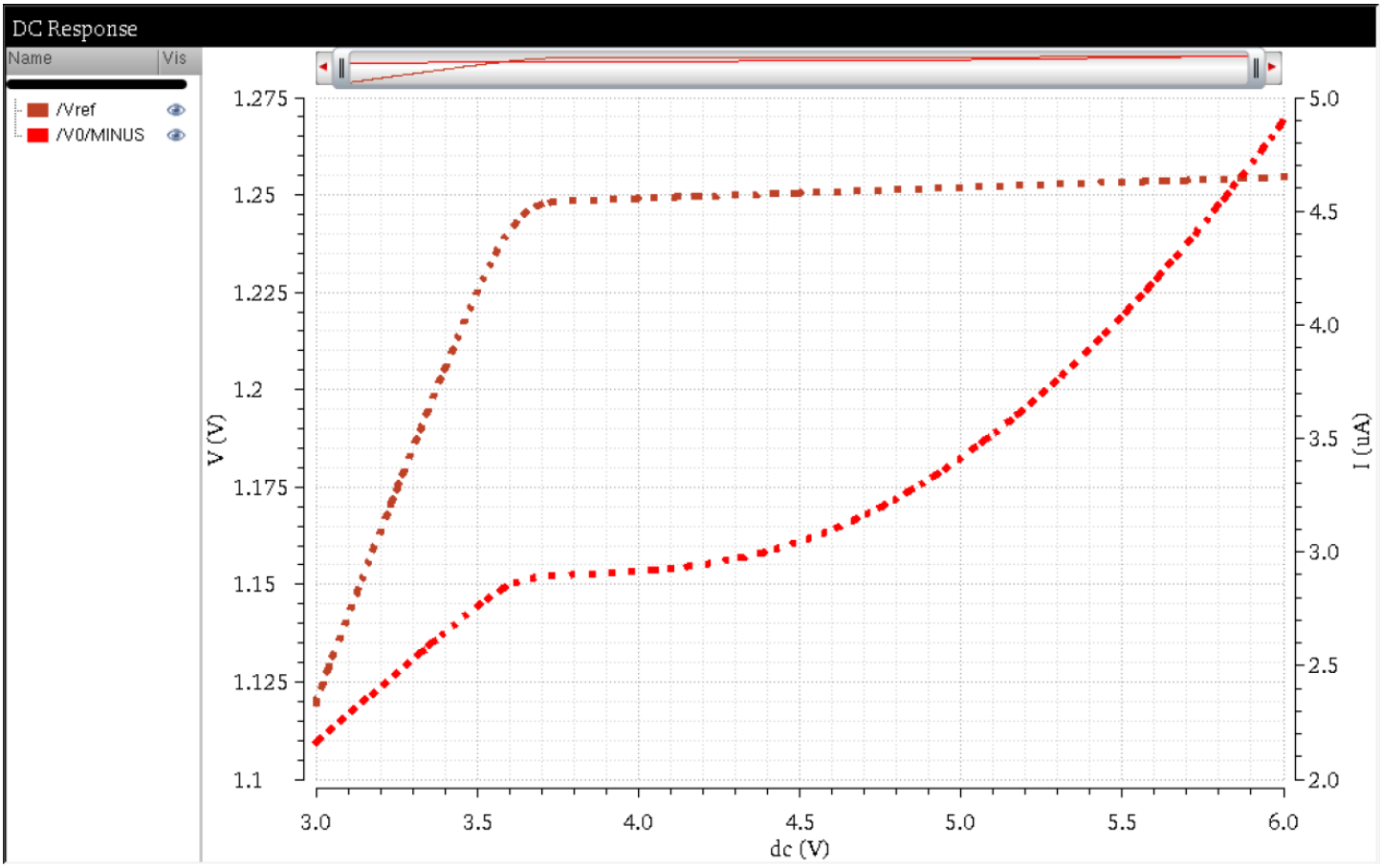
Bandgap Voltage Reference Schematic:



Bandgap Vref Vs. Increasing VDD:

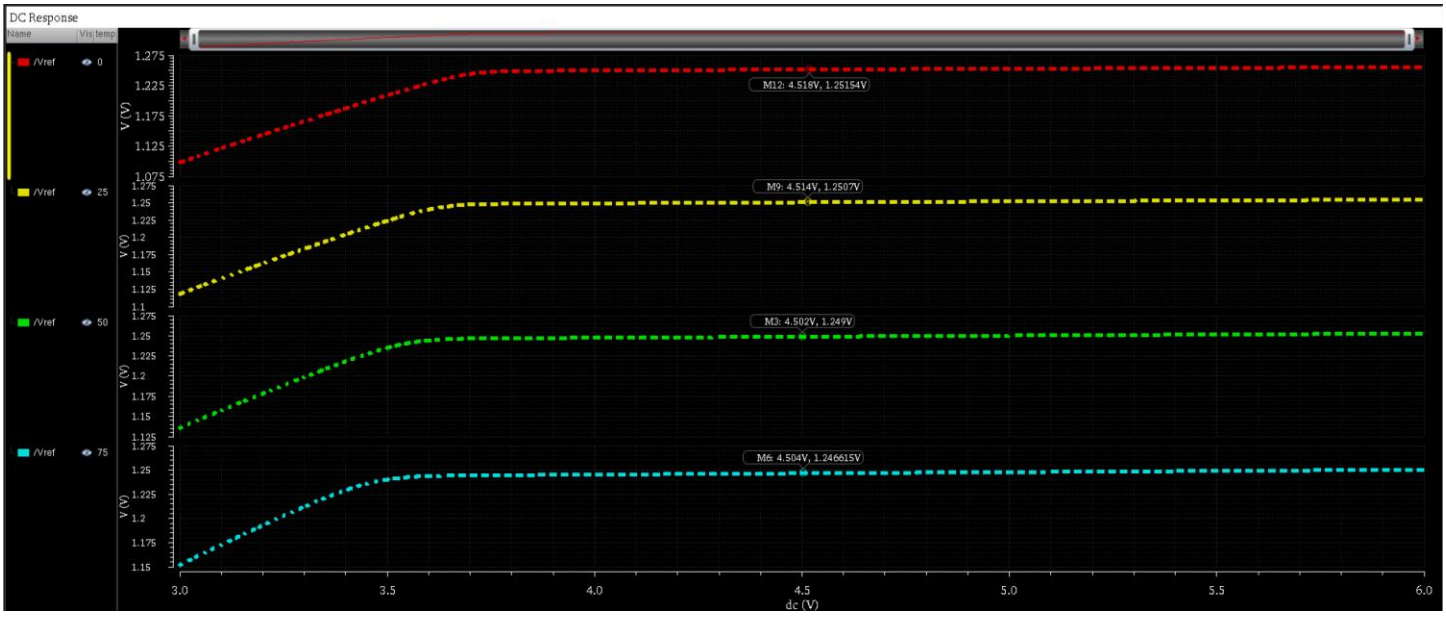
We will now test the bandgap against a change in VDD which is the overall power supply voltage to the device.





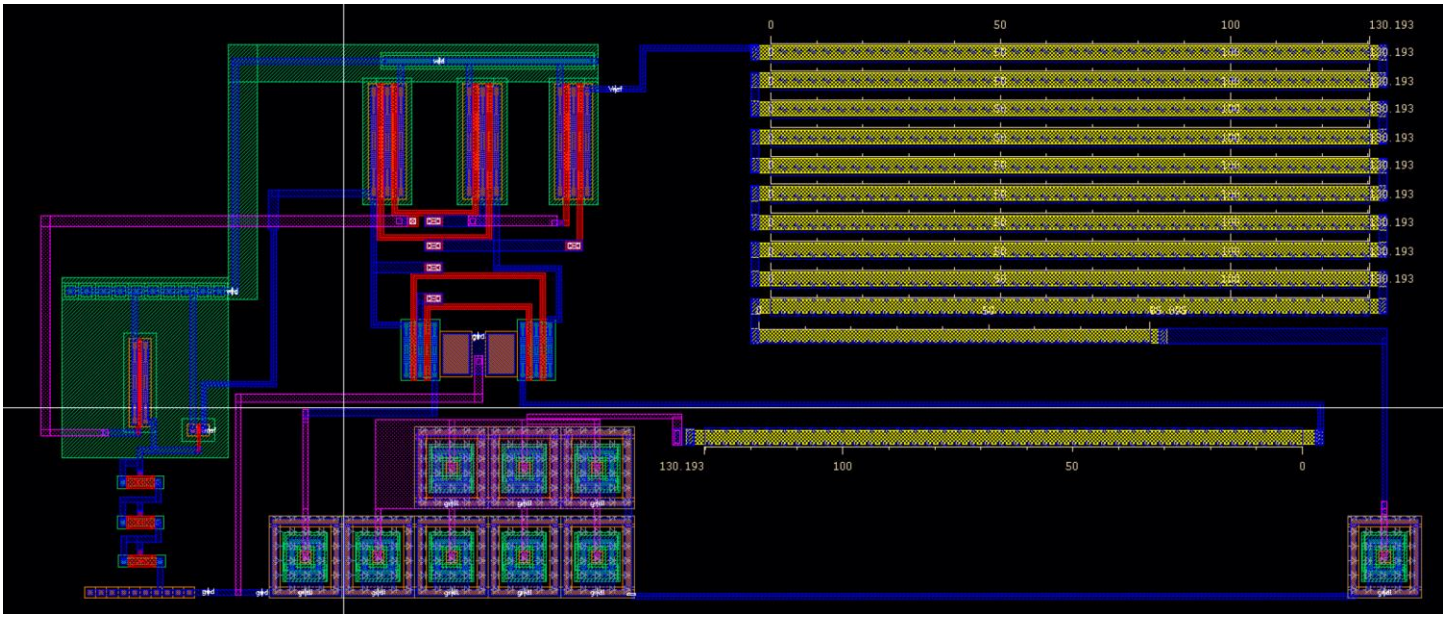
The bandgap shows a gradual increase in the reference voltage as the supply voltage is increased. This is an important consideration as this means that for higher values of Vref we will also obtain higher values of Vout from the Boost SPS.

Bandgap Vref Vs. Increasing Temperature and Increasing VDD

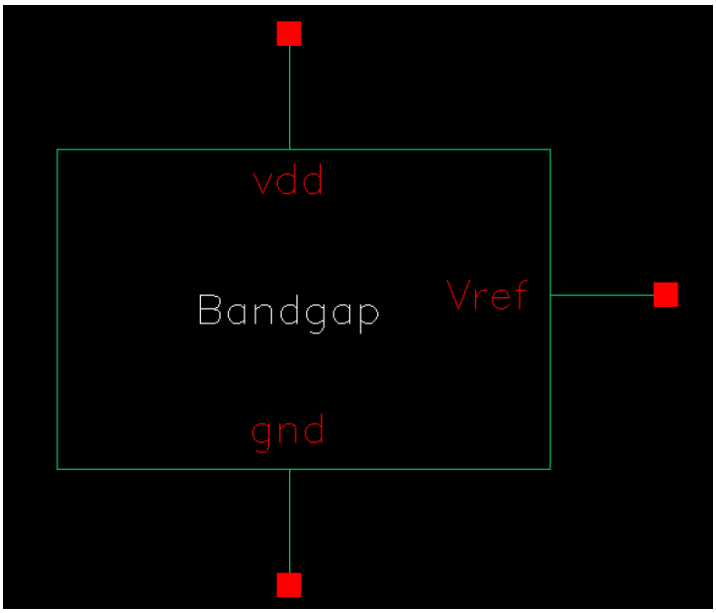


As with the simulation conducted with the diode, we are testing the reference voltage of the bandgap vs. changes in temperature. The reference voltage decreases as the temperature increases from 0 to 75 degrees Celsius with a max change of roughly 15mV. At room temperature the voltage reference sits at 1.2507V, which is ideal for the operation of this device.

Bandgap Reference Layout:



Bandgap Reference Voltage Symbol



Part 2: Comparator

The comparator takes in the feedback voltage and compares it with the reference voltage of 1.25V. If the feedback voltage is lower than 1.25V then the comparator will output a logic low (0V) signal. If the feedback voltage is higher than 1.25V then the comparator will output a logic high (VDD) signal.

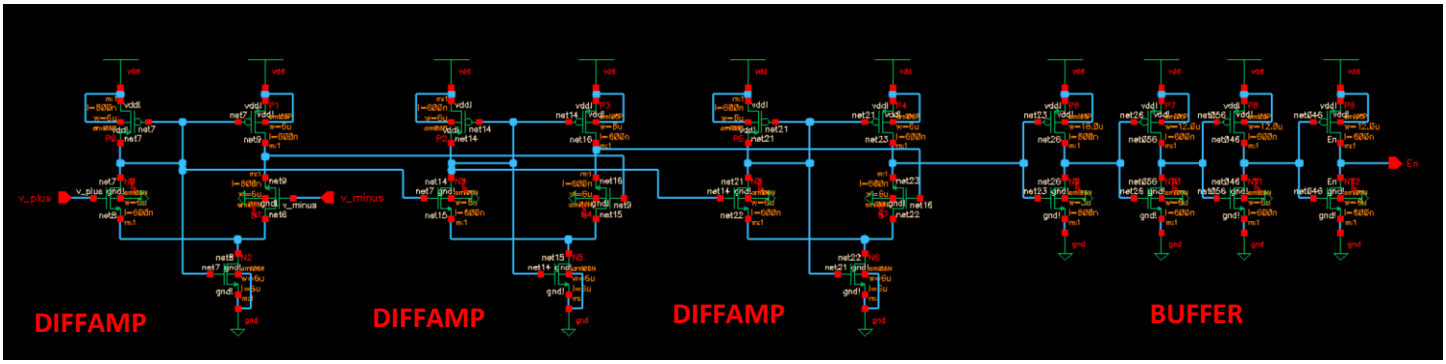
The comparator is composed of three cascaded diff-amp circuits plus buffering stages to better drive the enable signal. The NMOS and PMOS sizes were selected to have a ratio of 10/1 (W/L) for each of the transistors. The effects of this choice allow for the design to consume less power given the following relation:

$$Rn = Rn' * \frac{L}{W} = 20k * \frac{1}{10} = 2k$$

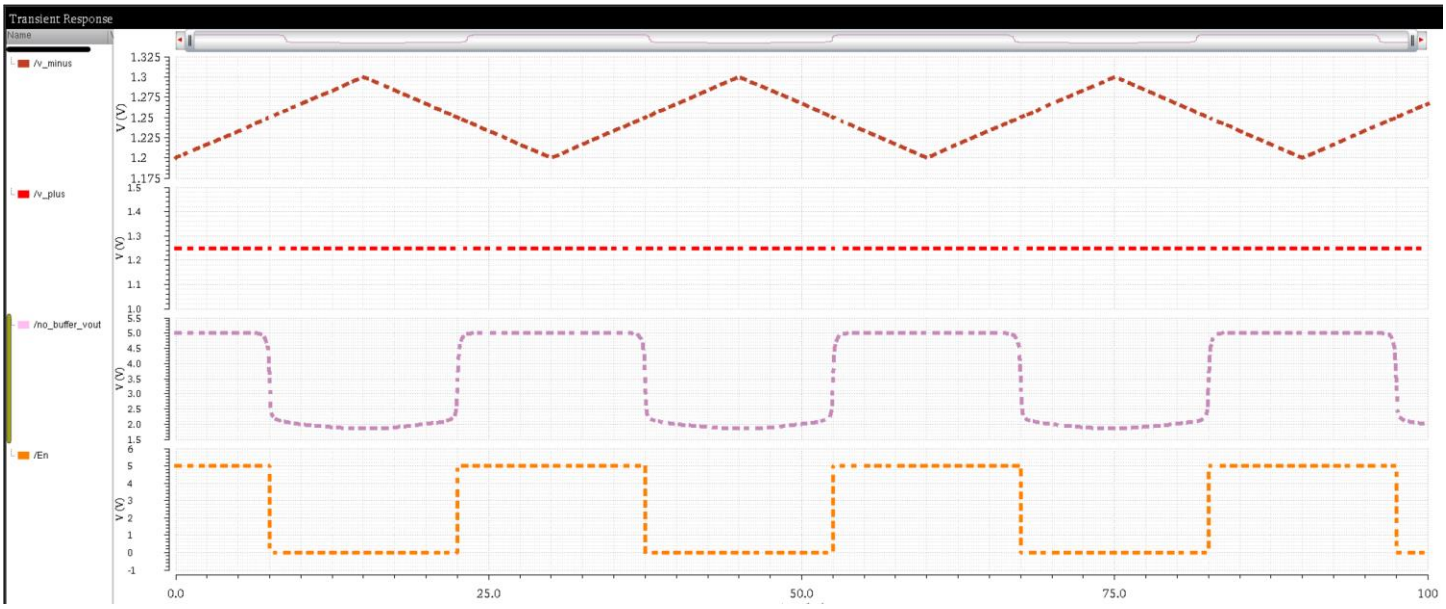
$$Rp = Rp' * \frac{L}{W} = 40k * \frac{1}{10} = 4k$$

The higher switching point resistance for the PMOS allows less current to flow through and therefore dissipates less power. However, a consequence of this design choice will the shift in the voltage switching point which will need to be corrected using an inverter in the buffering stage (more specifically the first inverter) to control the switching point. The combination of the decreased PMOS body sizes and the switching point controller will still result in lower power consumption, overall. Much of the design for this comparator was taken from the CMOS textbook.

Comparator Schematic:

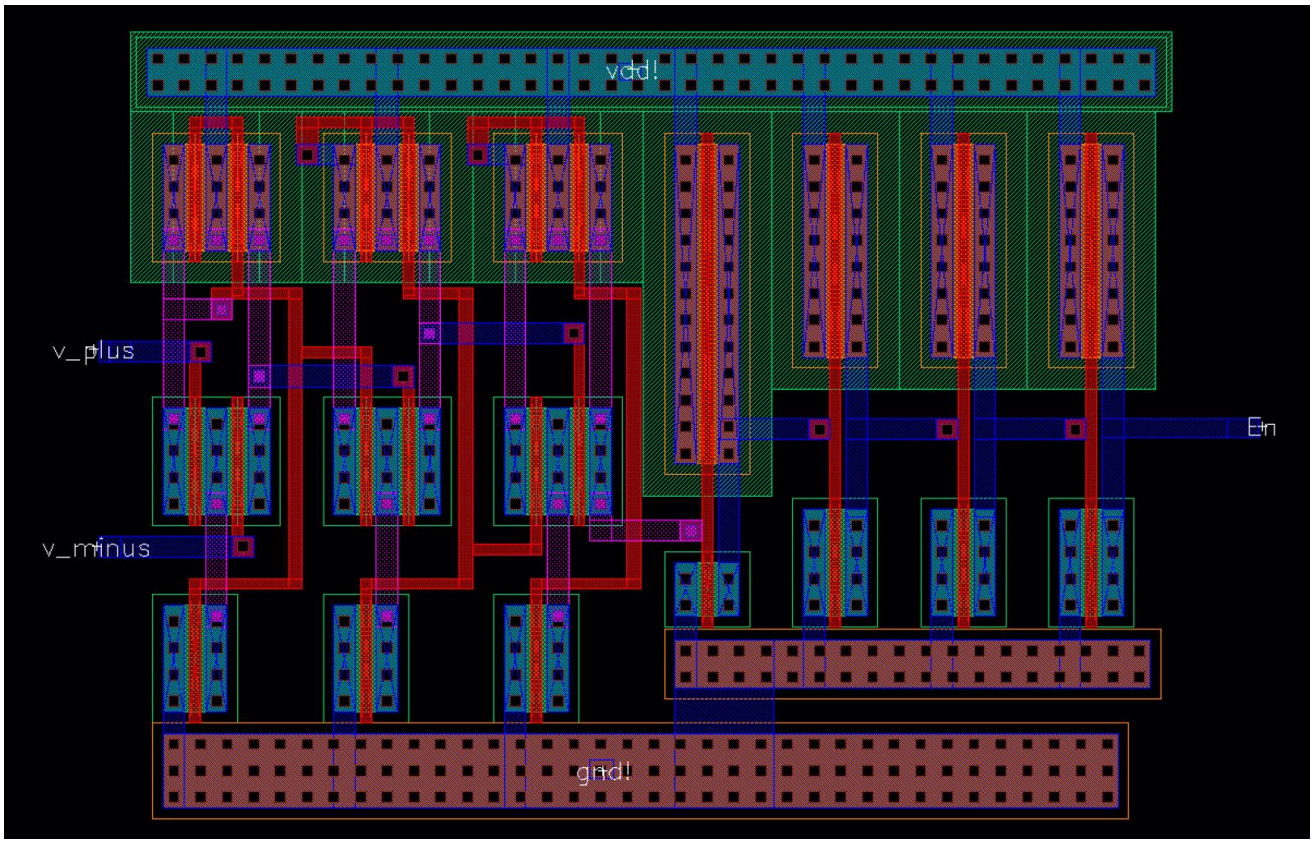


Comparator Simulation:

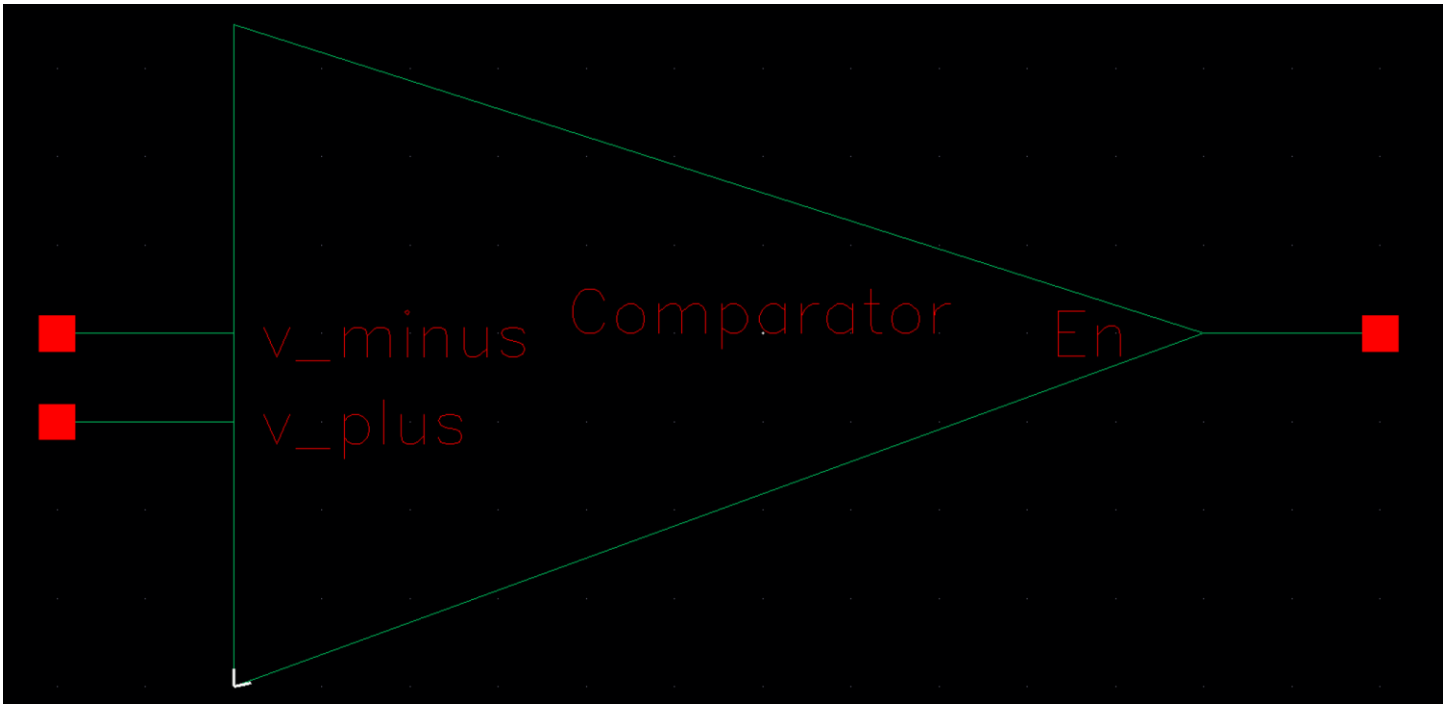


In this simulation, v_minus is the signal that is being compared against v_plus. During the points where v_minus crosses above 1.25V we can see the enable signal turned off. However, we see that for the instances where v_minus is below 1.25V that the enable signal is turned on. We can also see the effects of the buffer as the non-buffered enable signal is rounded. The buffer produces a sharper edge for a clearer enable toggle.

Comparator Layout:



Comparator Symbol:

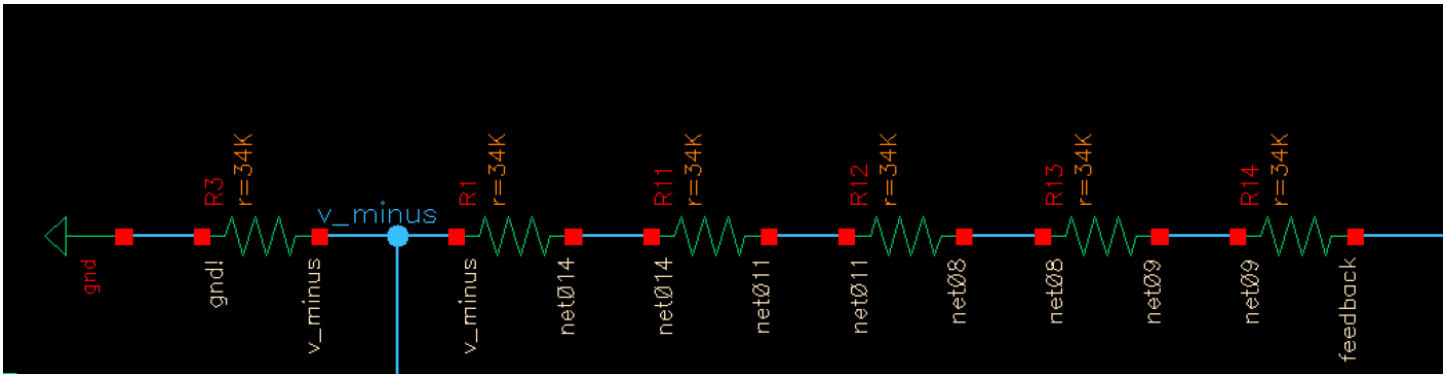


Part 3: Feedback Voltage Divider

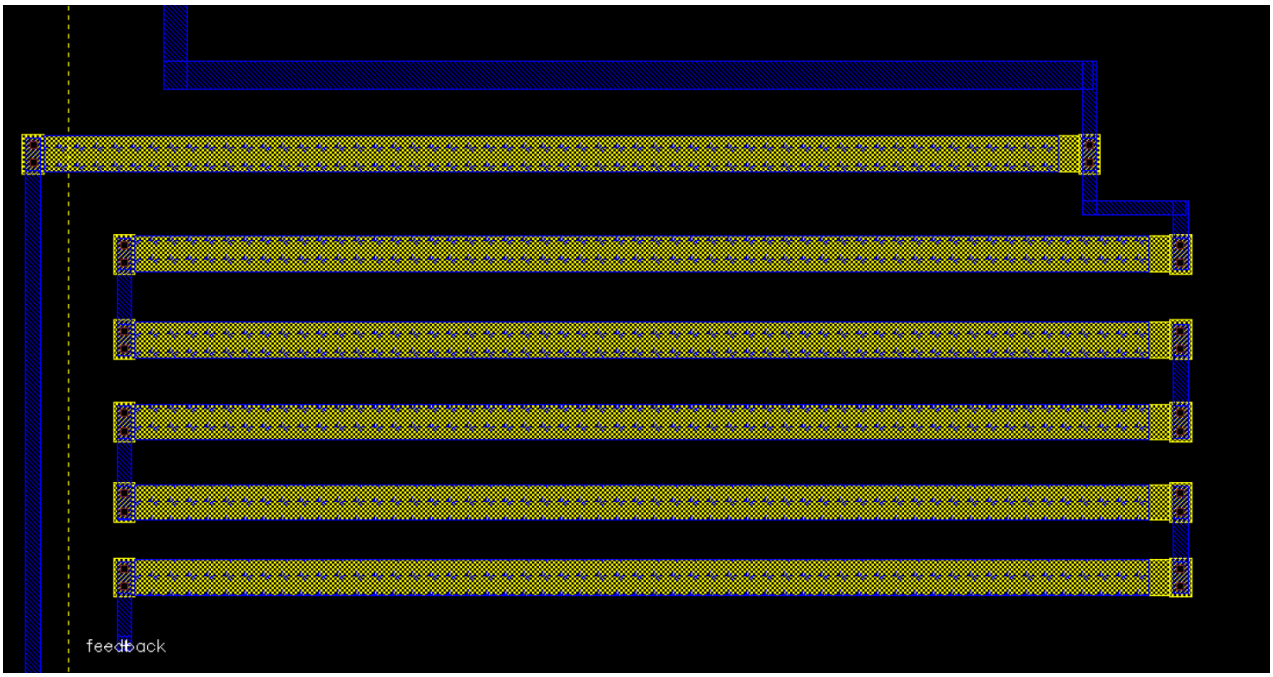
The feedback voltage divider takes the output signal of the Boost SPS and feeds it into the comparator. The expected output voltage for the divider is 7.5V so the voltage needs to be divided by a factor of six for it to be properly compared against the 1.25V voltage reference produced by the bandgap circuit. 34K Resistors were chosen through trial and error to produce a reasonable amount of current through the feedback, which for the design specifications must be between 10uA and 50uA. Given an output voltage of 7.5V the compared voltage can be calculated as follows:

$$V = V_{in} * \frac{34k}{34k + 5 * 34k} = 7.5V * \frac{34k}{34k + 5 * 34k} = 1.25V$$

Voltage Divider Displayed in The Circuit:



Voltage Divider Layout



Part 4: Oscillator

The oscillator controls the overall frequency of the Boost SPS's operation. The component is made up of weak inverters assembled into a "ring oscillator". The whole device is enabled using a NAND gate to allow the comparator to toggle the oscillator on and off. The body size for the weak inverters was selected to be 6u/6u, which is a standard sizing the increases the amount of resistance of the inverter making them weaker.

The design parameters specified an oscillation frequency between 1MHz and 10MHz, so we will choose the median frequency of 5MHz. To calculate the frequency of this design we will need to find the delay between each inverter. To start we will find C'ox or Ctot.

$$R_n = R'_n * \frac{L}{W} = R'_n = 20k$$

$$R_p = R'_p * \frac{L}{W} = R'_p = 40k$$

$$C_{oxp} = C'_{ox} * W_p * L_p = \frac{2.5fF}{\mu m^2} * 6\mu^2 = 90fF$$

$$C_{oxn} = C'_{ox} * W_n * L_n = 90fF$$

$$C_{tot} = \frac{5}{2}(C_{oxp} + C_{oxn}) = \frac{5 * (180fF)}{2} = 450fF$$

Now we will use this capacitance to find the total delay between each inverter:

$$t_{PLH} = 0.7 * R_p * C_{tot} = 0.7 * 40k * 450fF = 12.6ns$$

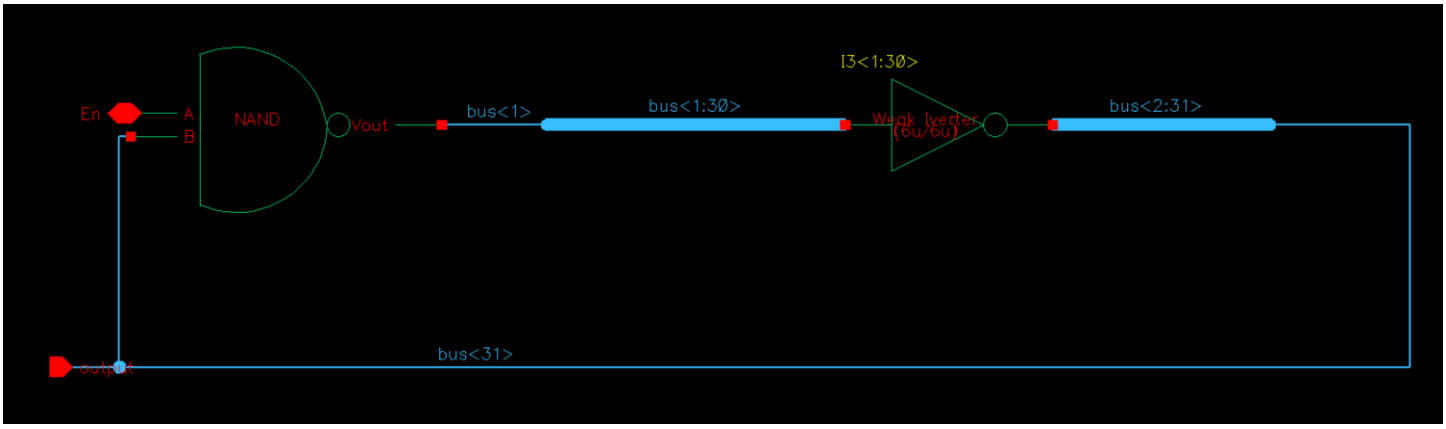
$$t_{PHL} = 0.7 * R_n * C_{tot} = 0.7 * 20k * 450fF = 6.3ns$$

Oscillation frequency is calculated as follows:

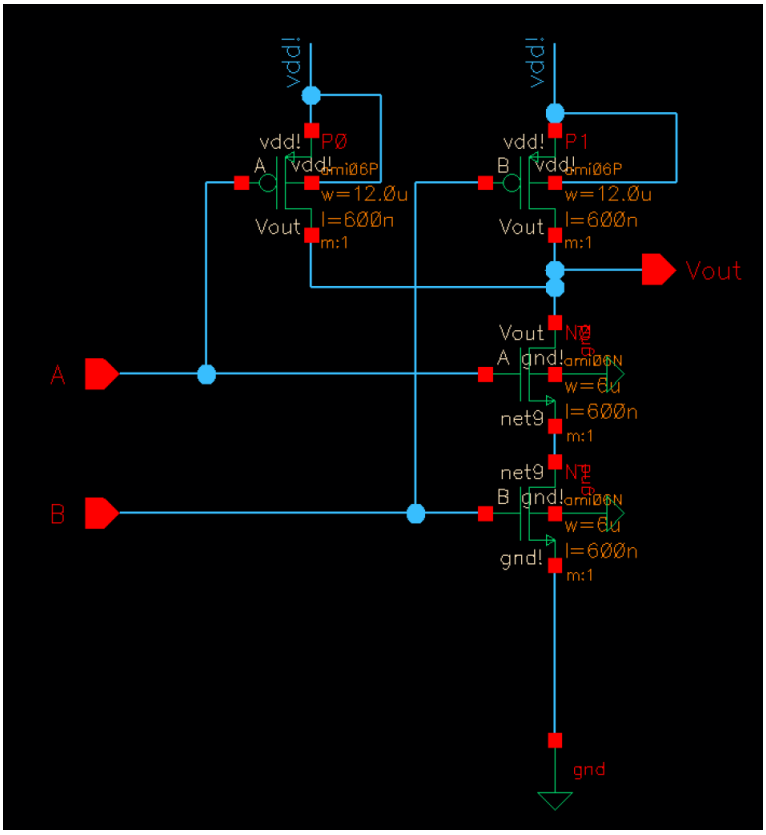
$$f_{osc} = \frac{1}{\frac{n}{2}(t_{PHL} + t_{PLH})} \rightarrow n = \frac{1}{\frac{fosc}{2} * (t_{PHL} + t_{PLH})} = \frac{1}{2.5MHz * (18.9ns)} = 21.2\ inverters$$

We will find through simulation that 21 inverters did not produce the desired frequency of 5MHz, so we bumped up the number of inverters until the frequency was reached. The inverters required were 31.

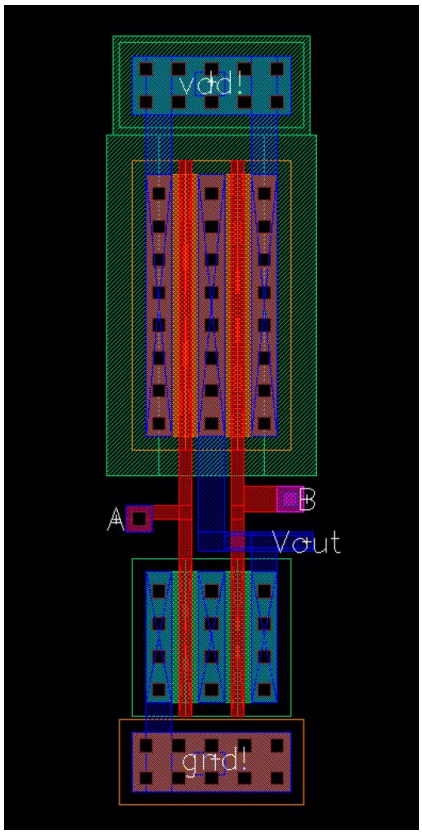
Oscillator Schematic :



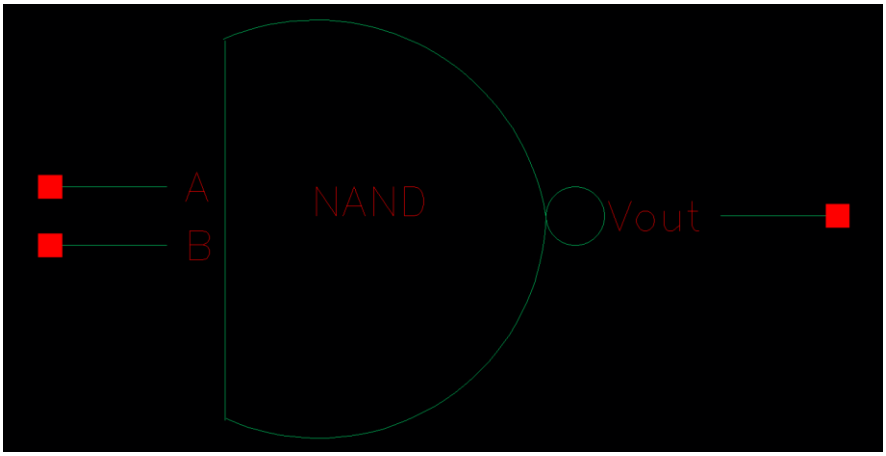
NAND Gate Shematic:



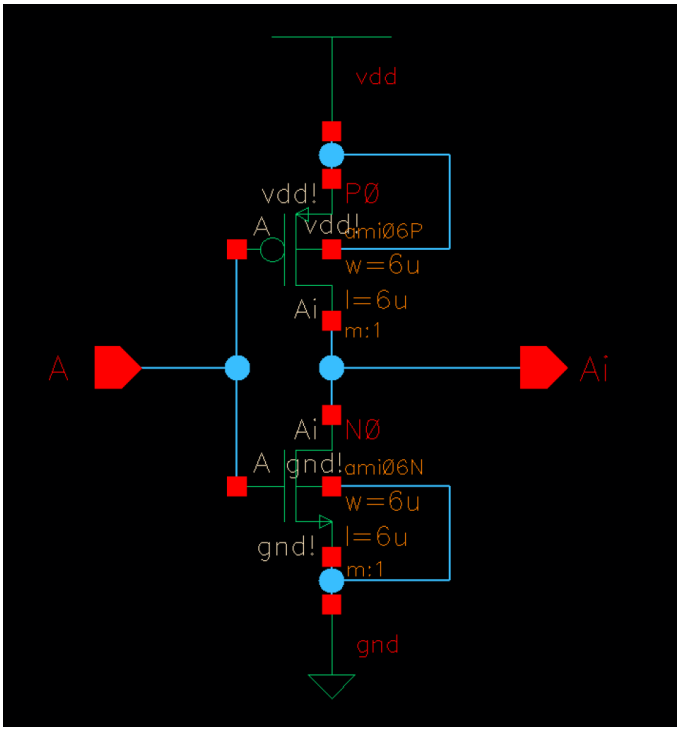
NAND Gate Layout:



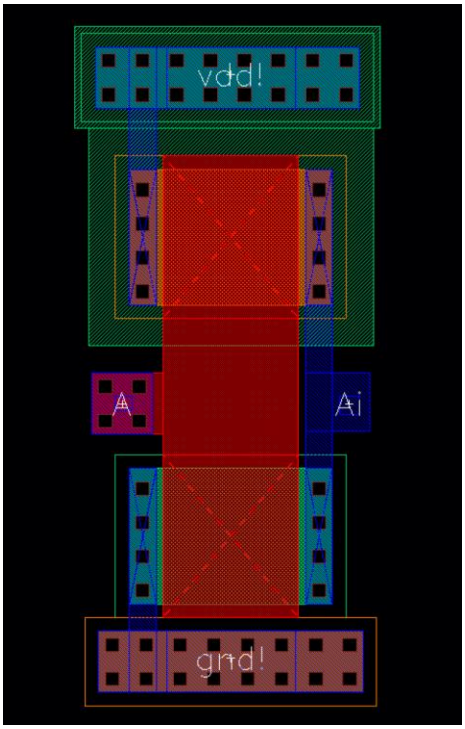
NAND Gate Symbol:



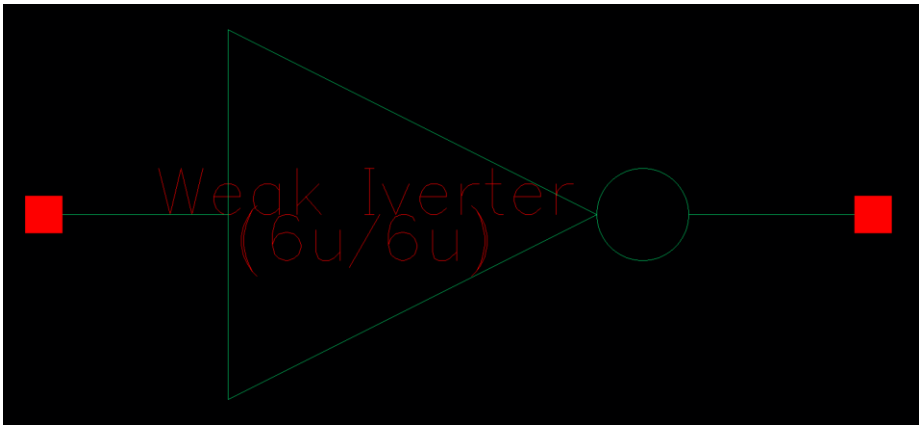
Weak Inverter Schematic:



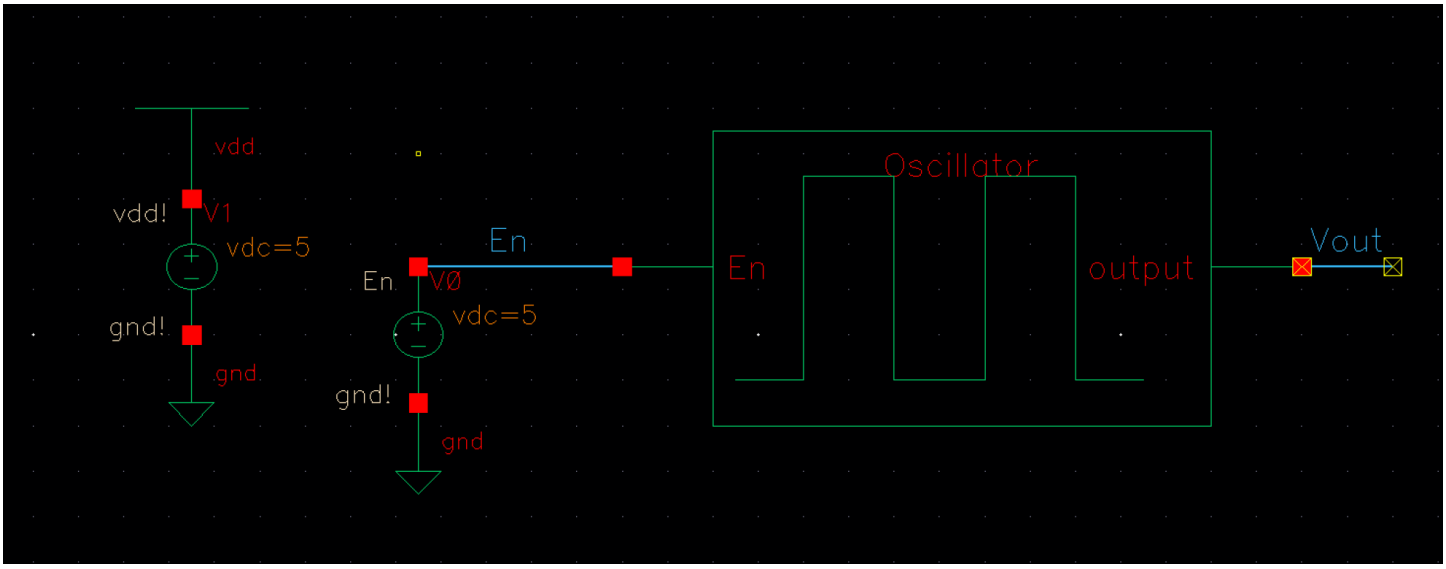
Weak Inverter Layout:



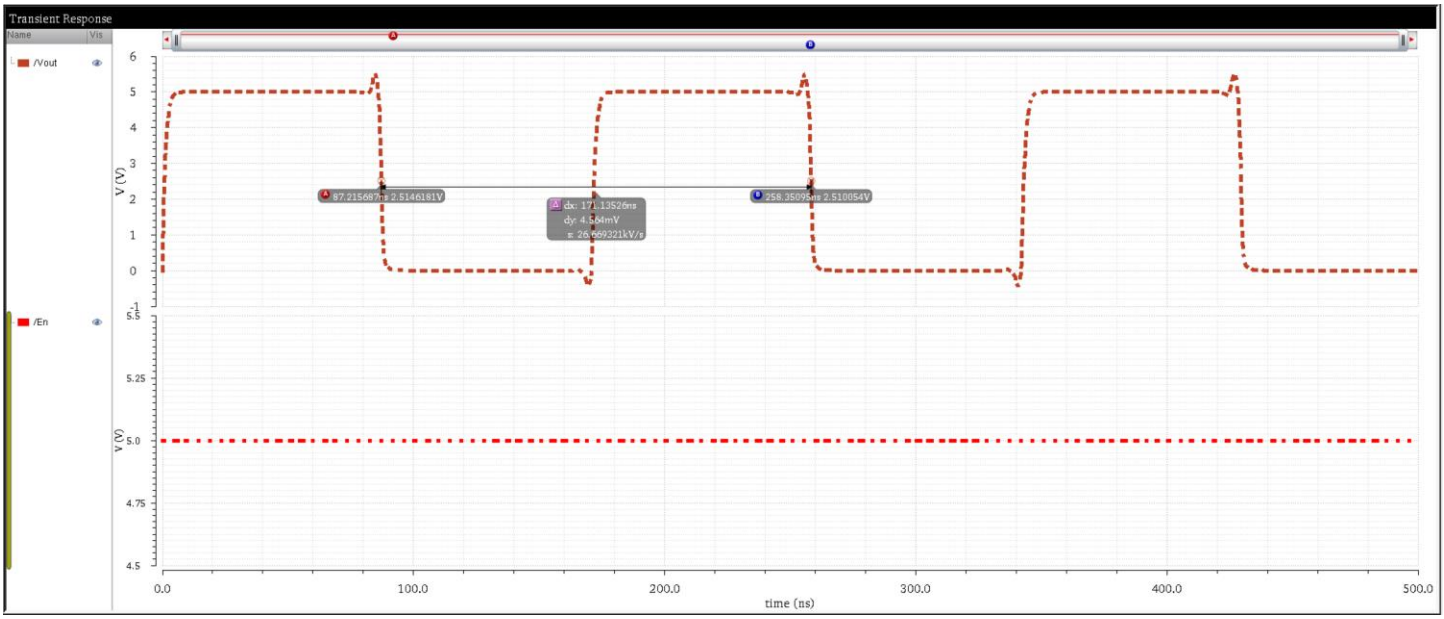
Weak Inverter Symbol:



Testing the Oscillator

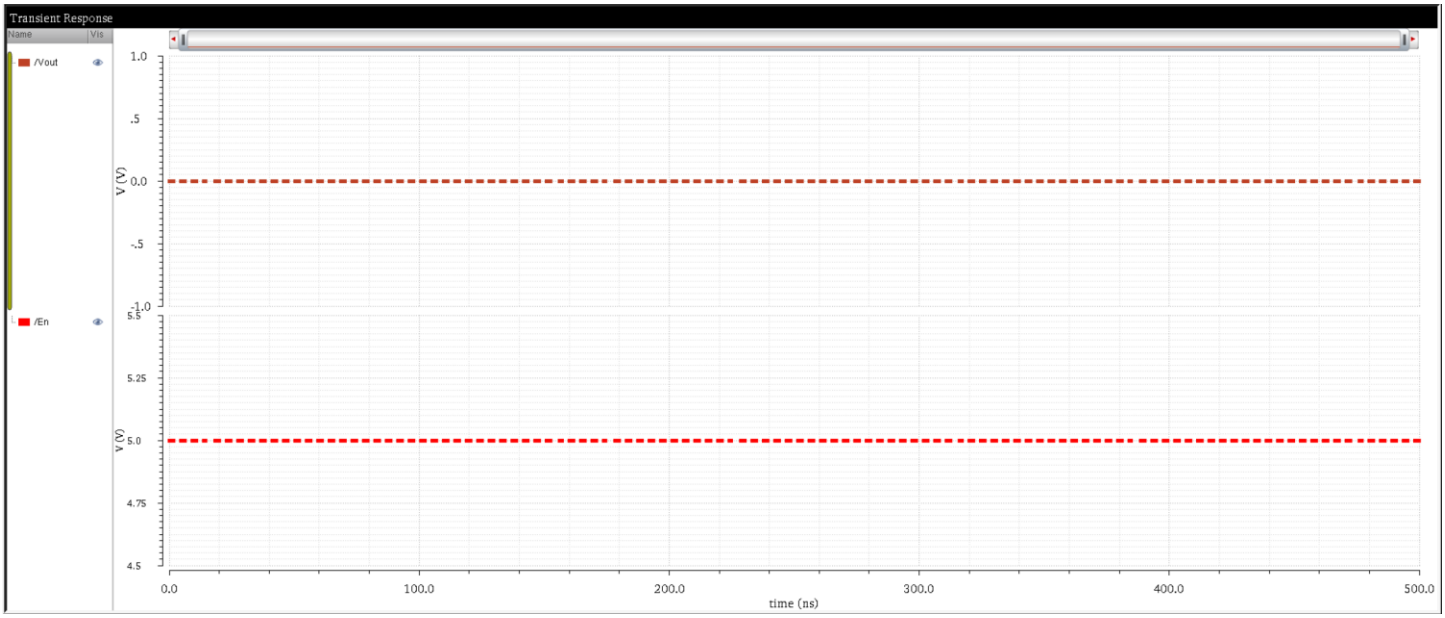


Enable on



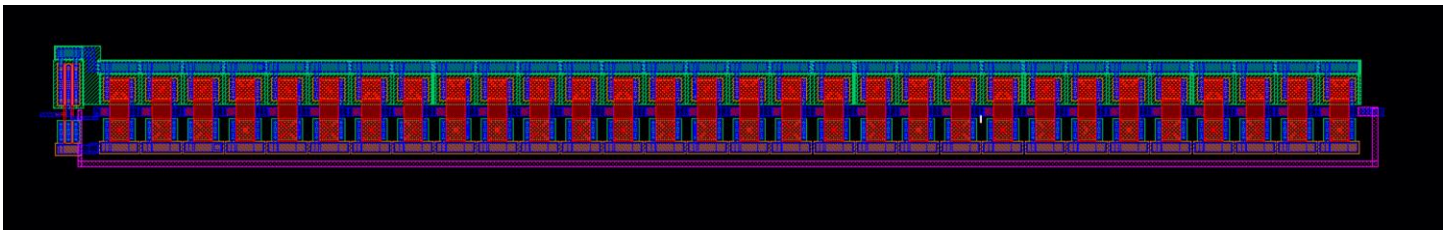
Testing the oscillator with the enable on produces a period of 171 ns, which equates to a frequency of 5MHz. This test shows that the oscillator is indeed controlled by the NAND gate.

Enable off

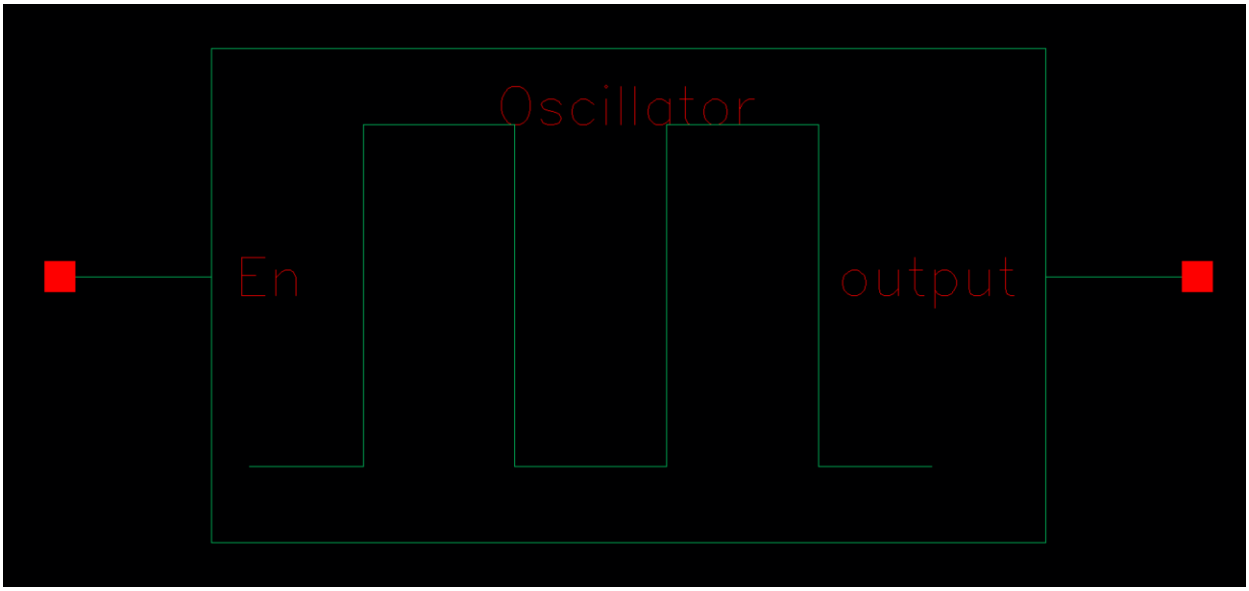


The oscillator also shuts off when the enable signal reads low, which is what we expected from this design.

Oscillator Layout



Symbol



Part 5: Buffer

The buffer will boost the signal from oscillator and allow it to drive the large NMOS switch that follows it. The NMOS switch carries a very low switching resistance due to its very large body, so in tandem with the boosted oscillator signal it will be able to switch very quickly and make up for the capacitance generated by the very large NMOS switch. As a rule of thumb choosing stages to be multiples of 8 times the first stage is preferred, so the second stage is 8 times the first and the third stage will be 64 times the first stage in this design.

The number of stages were calculated using the following equation:

$$N(lnA) = \ln\left(\frac{C_{load}}{C_{in}}\right)$$

$$C_{load} = C'_{ox} * WnLn = \frac{2.5fF}{\mu m^2} * 3072 * 0.6\mu m = 4.6pF$$

Now we must find Cin

$$C_{oxn} = C'_{ox} * WnLn = \frac{2.5fF}{\mu m^2} * 6\mu m^2 = 9fF$$

$$C_{oxn} = C'_{ox} * WnLn = \frac{2.5fF}{\mu m^2} * 6\mu m * 12\mu m = 18fF$$

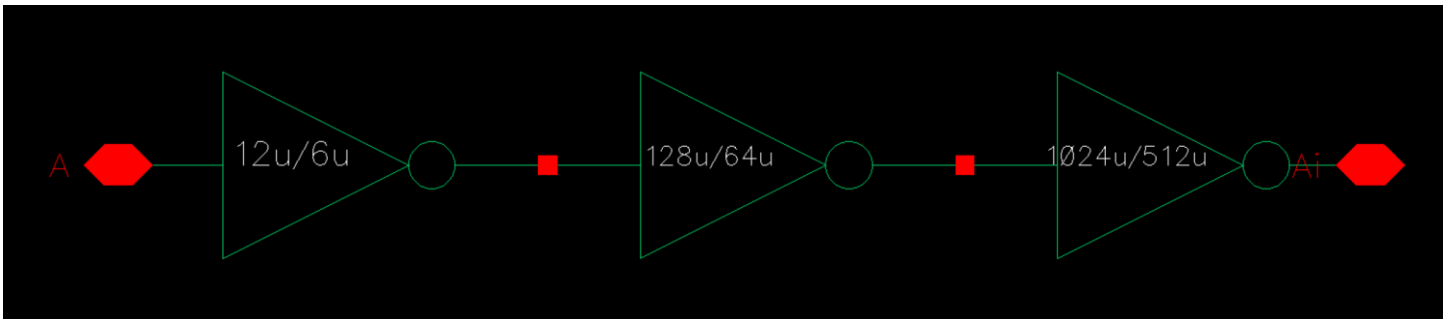
$$C_{in} = \frac{3}{2}\left(C_{oxn} + C_{oxp}\right) = \frac{3}{2}(9fF + 18fF) = 40.5fF$$

Which leads to the final calculation of

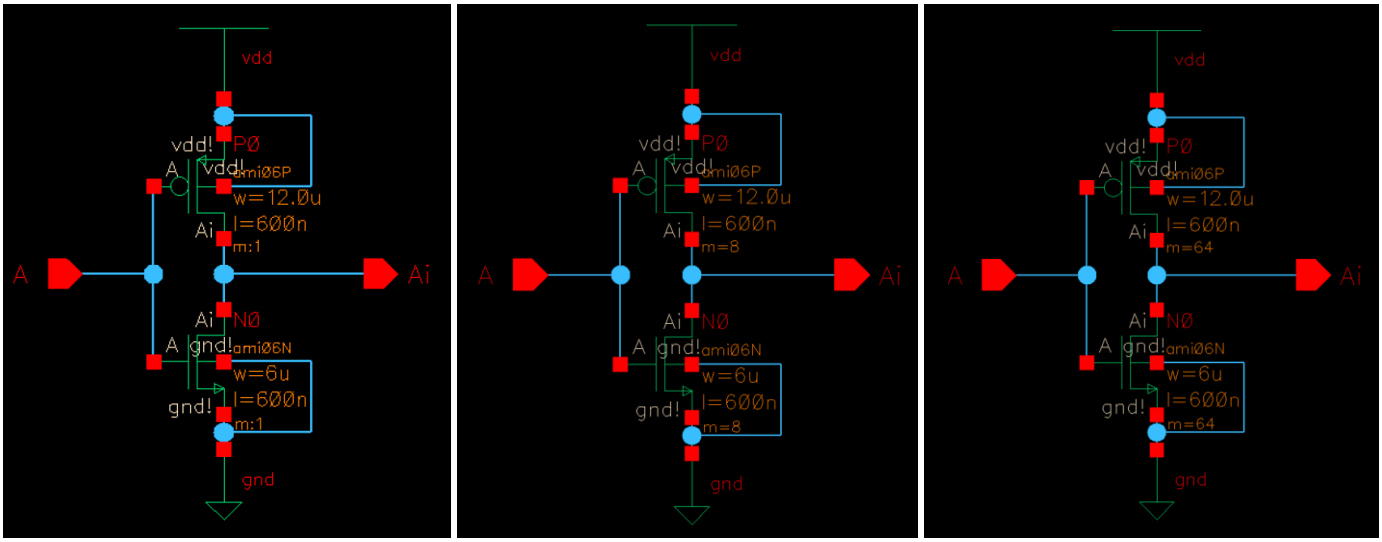
$$N = \frac{1}{2}\left(\ln\frac{4.6pF}{40.5fF}\right) = 2.368$$

This will be rounded up to 3 stages total.

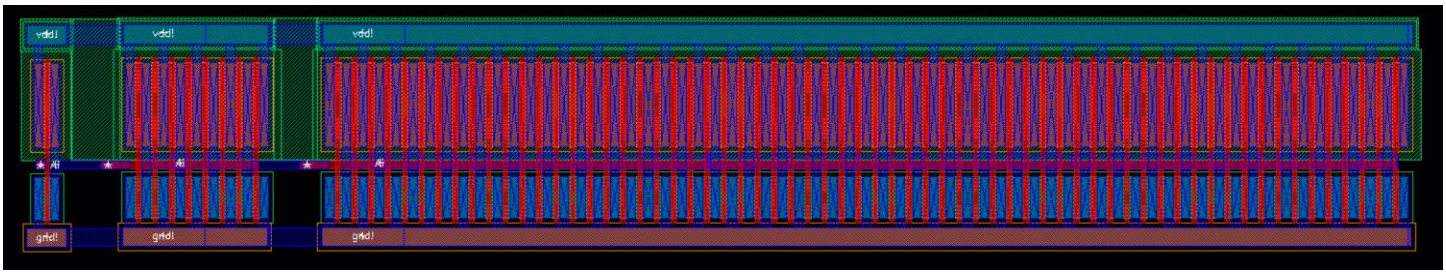
Buffer Schematic:



The Three Buffer Stages (individual schematic view first stage, 8x first stage, 64x first stage):



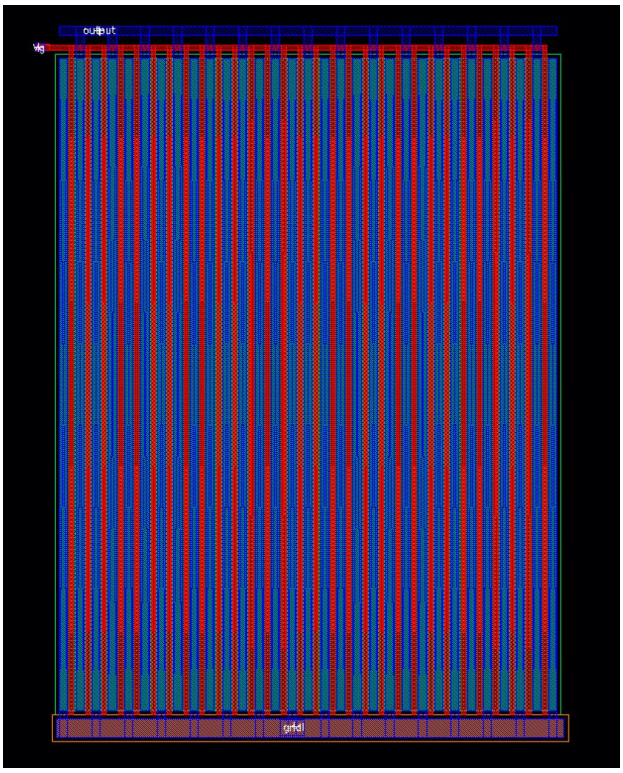
Buffer Layout:



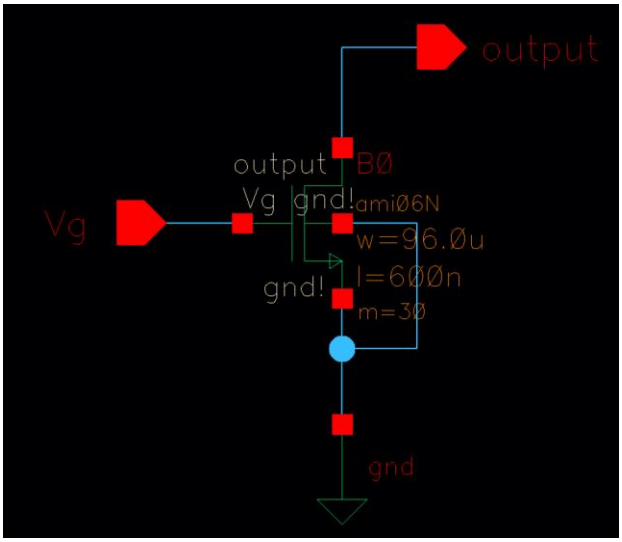
Part 6: NMOS Switch

As stated in the previous section, we will be using an NMOS switch that connects the on-board components to the off-board components. The NMOS switch is simply an NMOS with a very large width. The large width creates a very low resistance connection between our components.

NMOS Switch Layout:



NMOS Schematic:



Part 7: Off-chip Components (load resistor, capacitor, inductor, Schottky diode)

Load Resistor Selection:

The resistor was selected as to have a load current of 20mA as the project parameters specify not having a load current greater than 20mA. We want the device to be able to provide 7.5V under these constraints, so the resistor was calculated with the following calculation:

$$V = \frac{I}{R} \rightarrow R = \frac{I}{V} = \frac{20mA}{7.5V} = 375\Omega$$

Capacitor Selection:

$$C_{min} = \frac{Delay}{R * freq * (\frac{\Delta V_{out}}{V_{out}})} = \frac{0.50}{375\Omega * 5.05MHz * (\frac{0.010V}{7.5V})} = 198nF$$

The Capacitor ended up being smaller than was required after testing. An acceptable performance of the device was found by using 5uF capacitor.

Inductor Selection:

The inductor needs to be selected to be able to provide enough current to the output and the NMOS switch is opened. Given our duty cycle of 50% determined from the topology of the oscillator. An appropriate inductor can be calculated with the following:

$$L = \frac{V_{out} * D * (1 - D)}{f * \Delta i_L} = \frac{7.5V * 0.50 * 0.50}{5MHz * 2mA} = 187uH$$

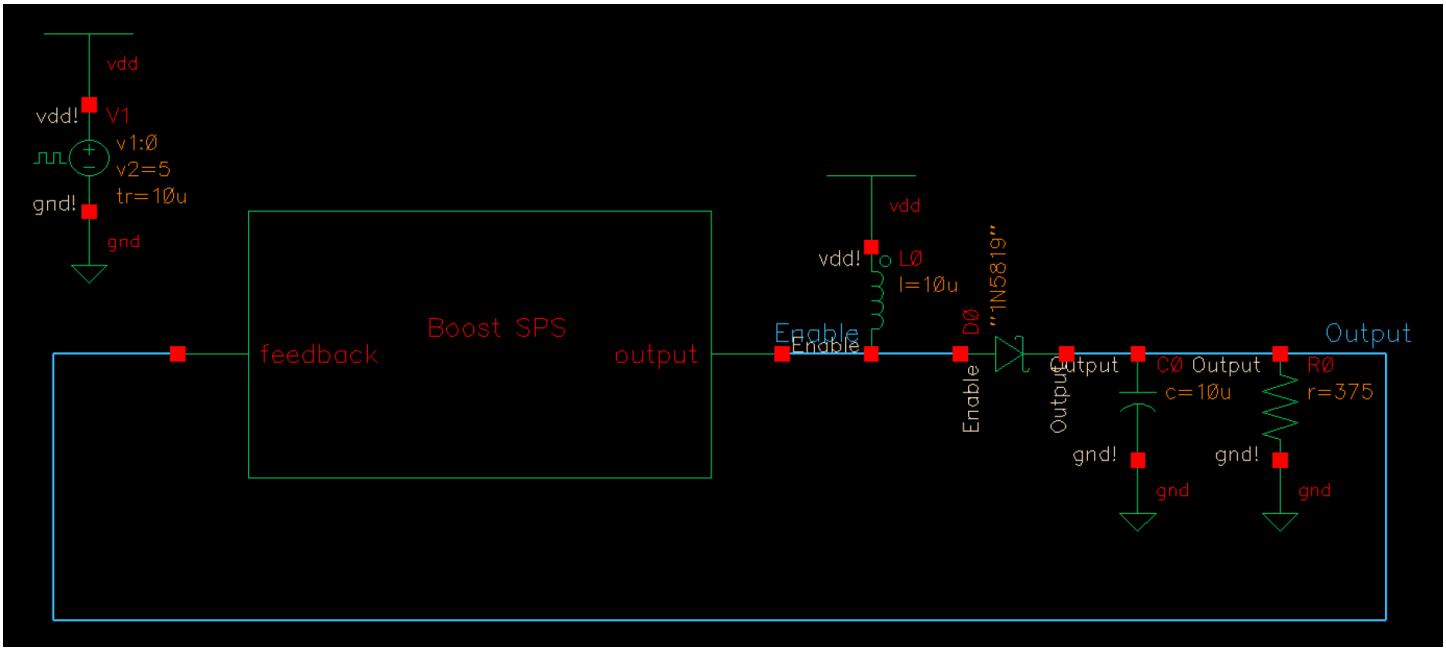
After testing, it was determined that a 10uH inductor would suffice

Schottky Diode Selection:

The Schottky diode used was the 1N5819, which was the example diode provided. We were advised to use other diodes due to the high capacitance associated with the diode (110pF), however after testing the operation of the boost sps I found that the diode can be used with the design.

Part 8: The Boost SPS Assembled and Tested

Simulation schematic



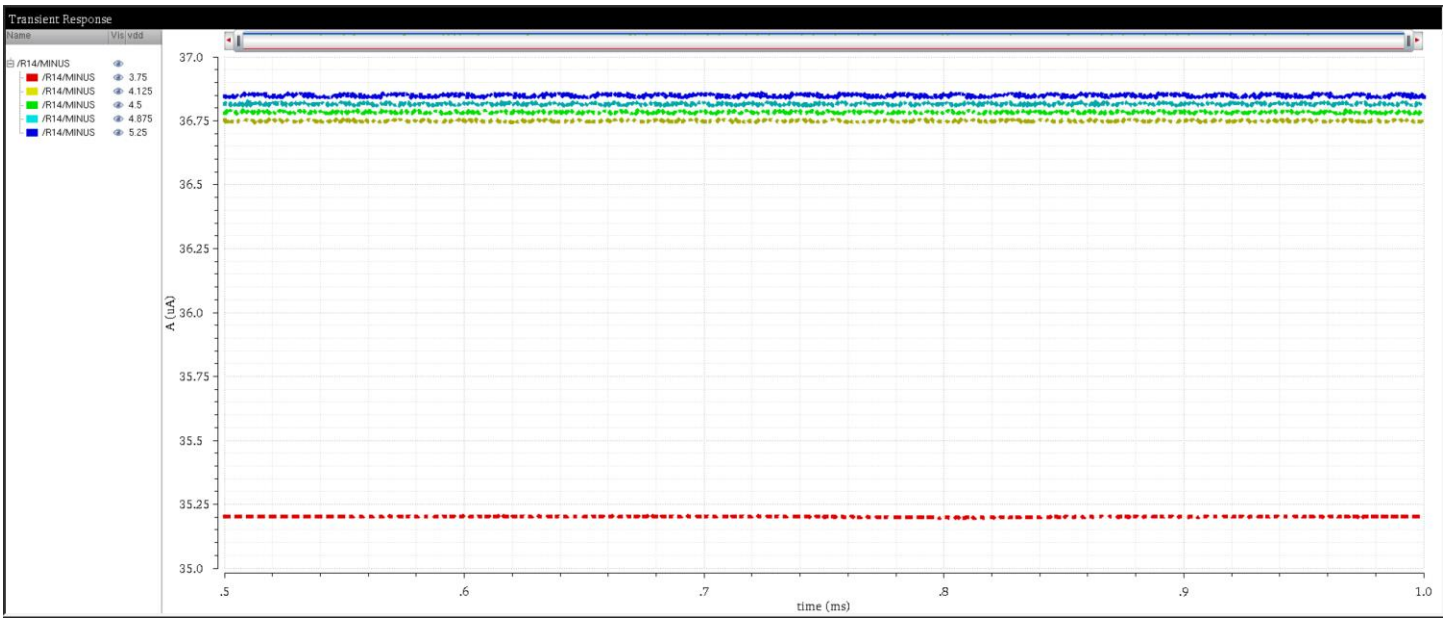
Device Efficiency:

The devices efficiency for most of the simulations ended up being above 90% in most cases along with varying temperatures and changes in VDD.

Efficiency can be calculated by determining the ration of the input power vs. the output power as follows:

$$Efficiency = E = \frac{Vout * I_{Load}}{VDD * I_{avg\ VDD}}$$

Source Current at Varying VDD



VDD 3.75V:

	Expression	Value
1	average(IT("/V...	39.21E-3

VDD 4V:

	Expression	Value
1	average(IT("/V...	40.28E-3

VDD 4.25V:

	Expression	Value
1	average(IT("/V...	38.19E-3

VDD 4.5V:

	Expression	Value
1	average(IT("/V...	36.35E-3

VDD 4.75V:

	Expression	Value
1	average(IT("/V...	34.59E-3

VDD 5V:

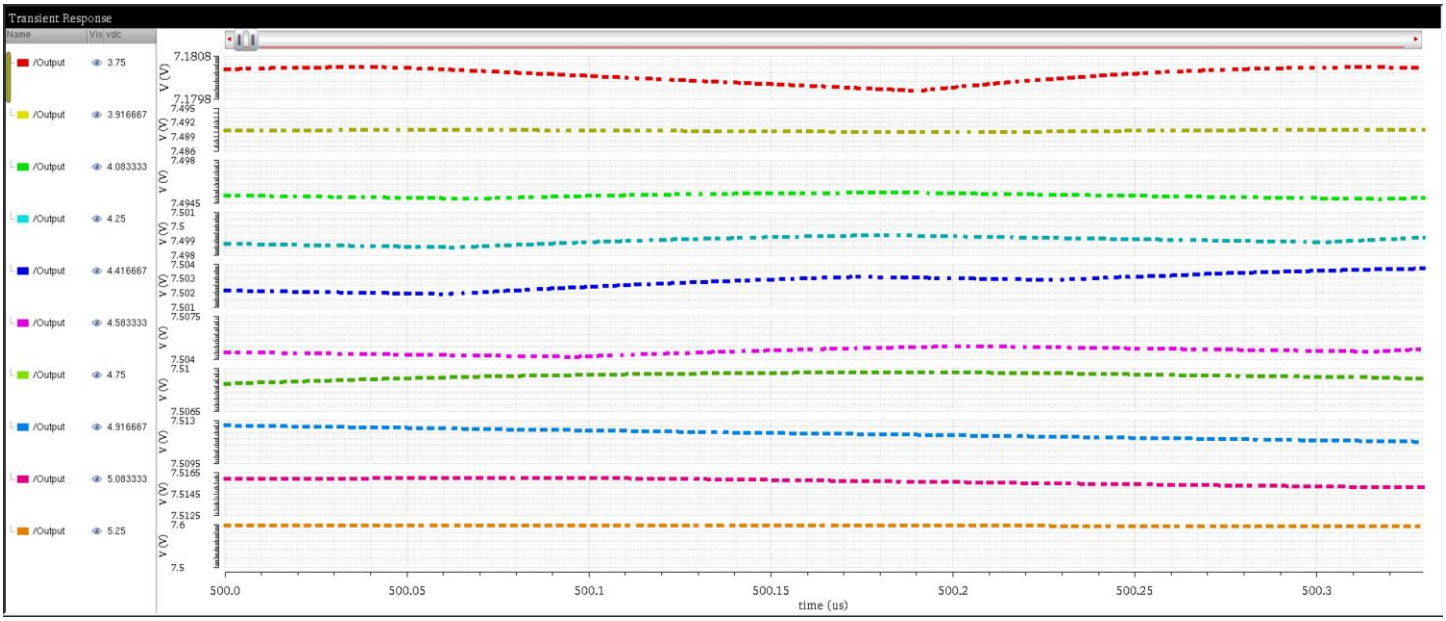
	Expression	Value
1	average(IT("/V...	33.16E-3

VDD 5.25V:

	Expression	Value
1	average(IT("/V...	30.55E-3

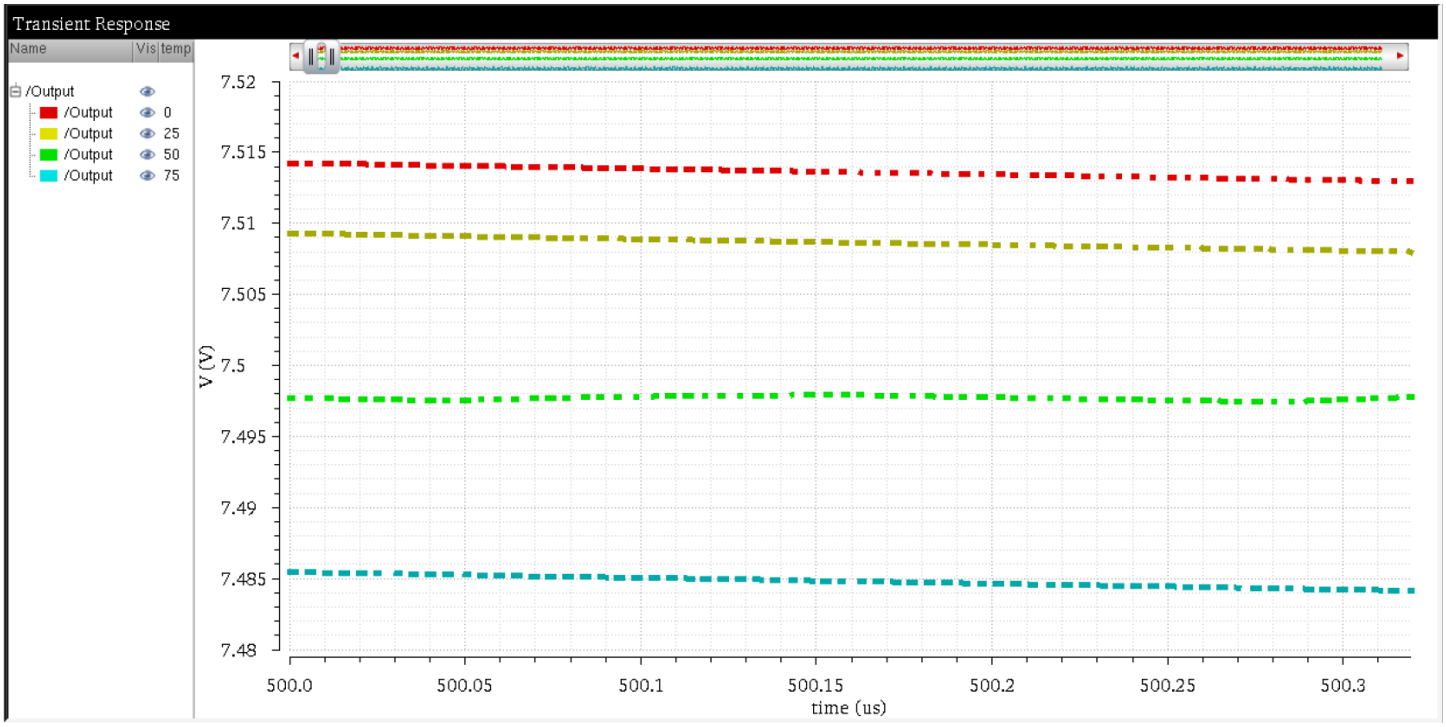
Efficiency at varying VDD		
VDD	Source current draw (A)	Efficiency
3.75	0.03921	1.020147921
4	0.04028	0.930983118
4.25	0.03819	0.924171711
4.5	0.03635	0.917010546
4.75	0.03459	0.912950199
5	0.03316	0.904704463
5.25	0.03055	0.935234978

Output Voltage vs. Varying VDD:

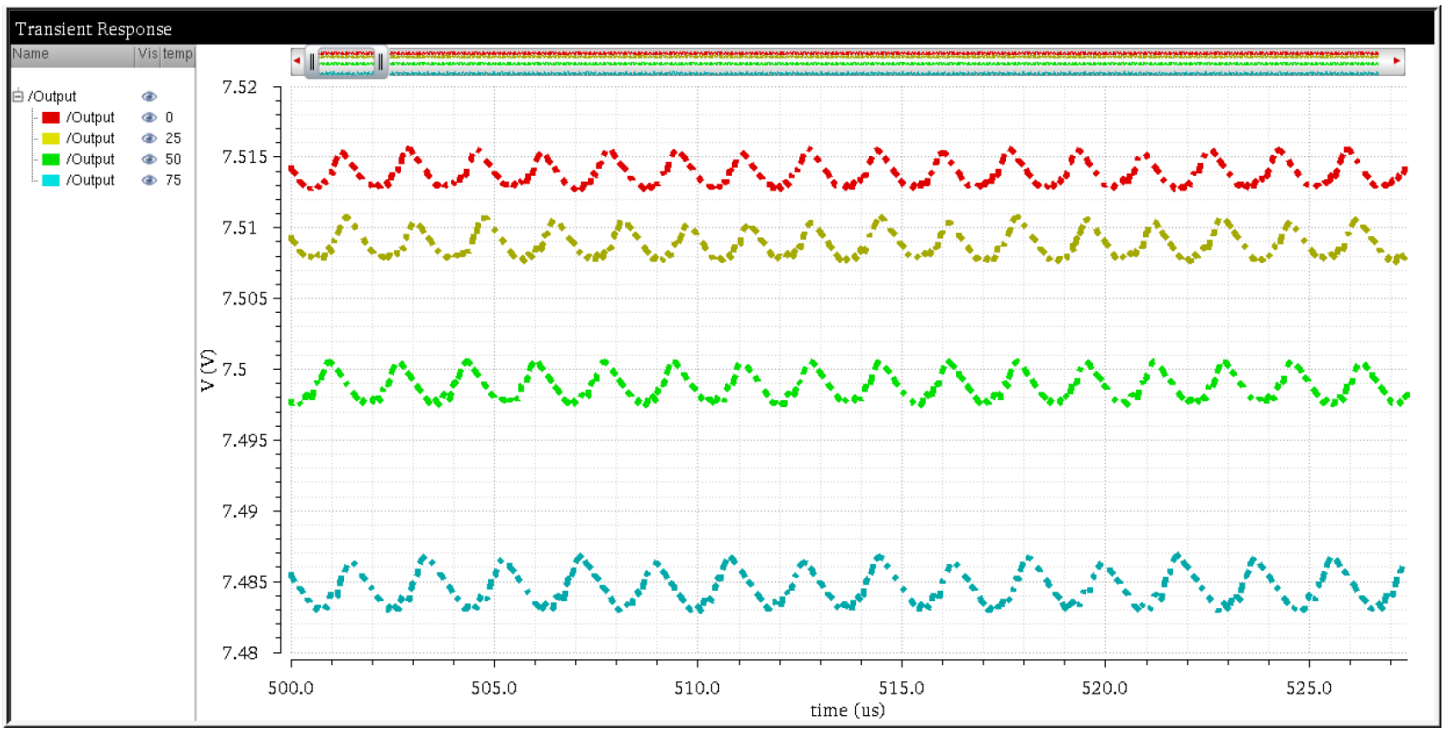


Output Voltage Vs. VDD	
VDD (V)	Output Voltage (V)
3.75	7.2
3.91	7.49
4.08	7.495
4.25	7.499
4.41	7.502
4.58	7.505
4.75	7.509
4.91	7.511
5.08	7.5165
5.25	7.55

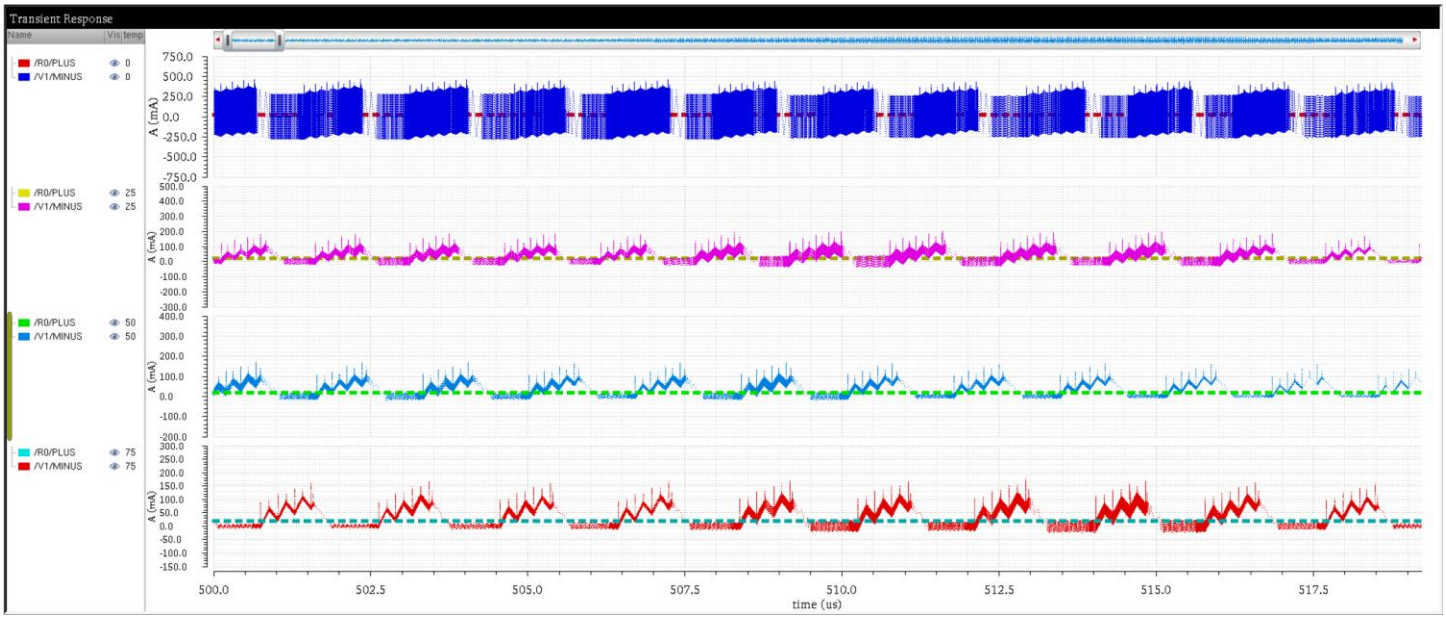
Temperature Testing for Vout:



Ripple Voltage at varying temperatures:



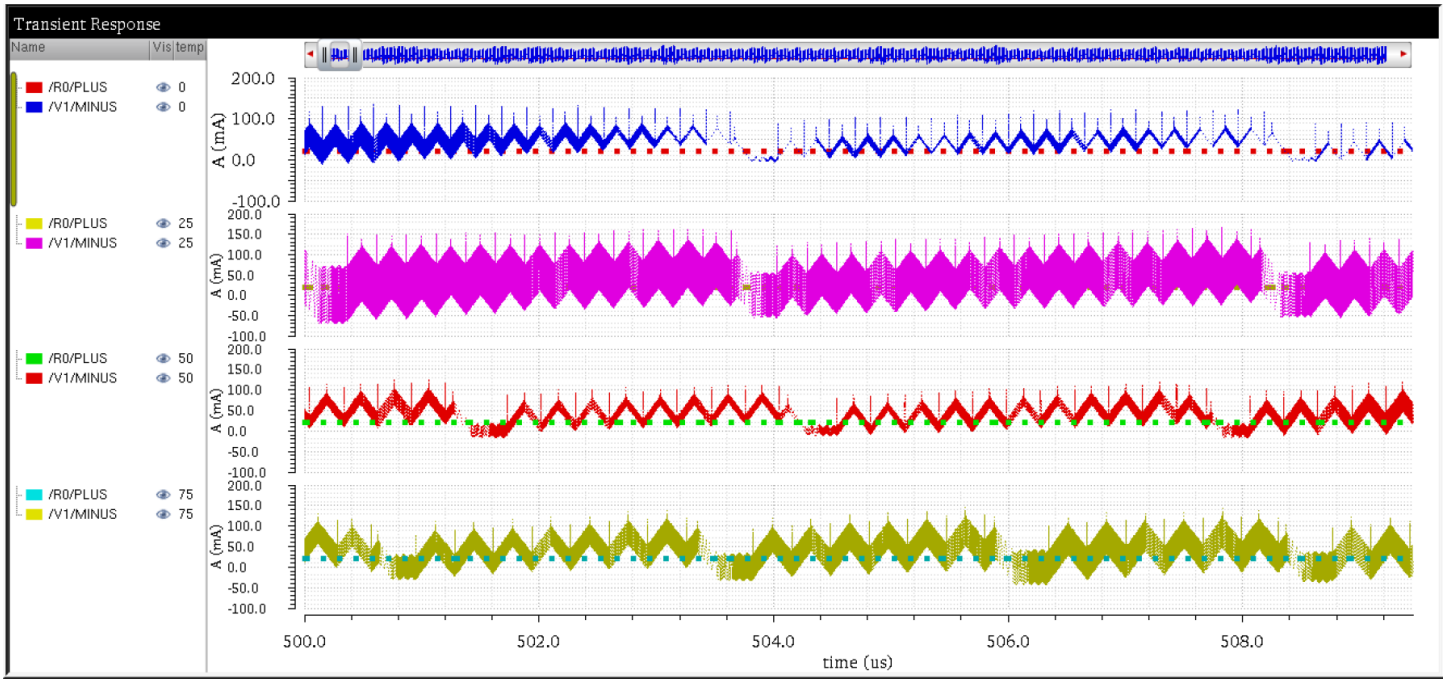
Load and Source Currents vs. Temperature (VDD = 4.75V):



Load and Source Currents at varying temperatures (VDD = 4.75V)

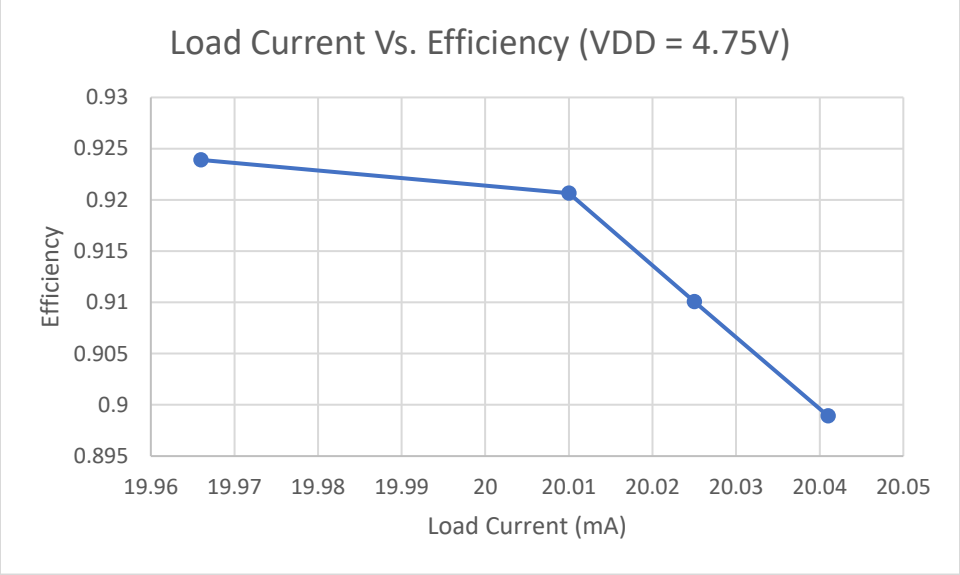
Temperature (celsius)	Load Current (uA)	Source Current (A)	efficiency
0	20.041	0.03513	0.898916805
25	20.025	0.0347	0.91005612
50	20.01	0.0343	0.920669019
75	19.966	0.03418	0.923901327

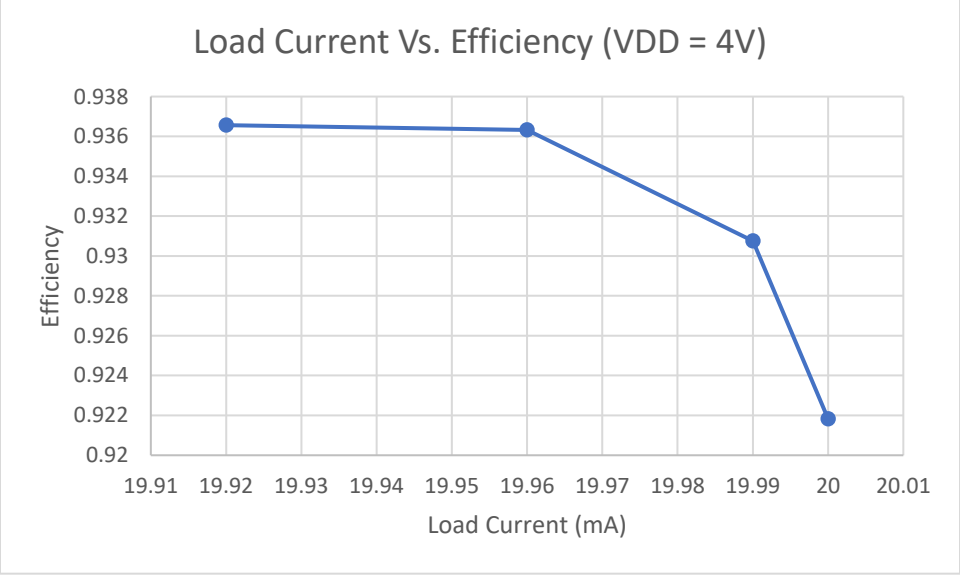
Load and Source Currents vs. Temperature (VDD = 4V):



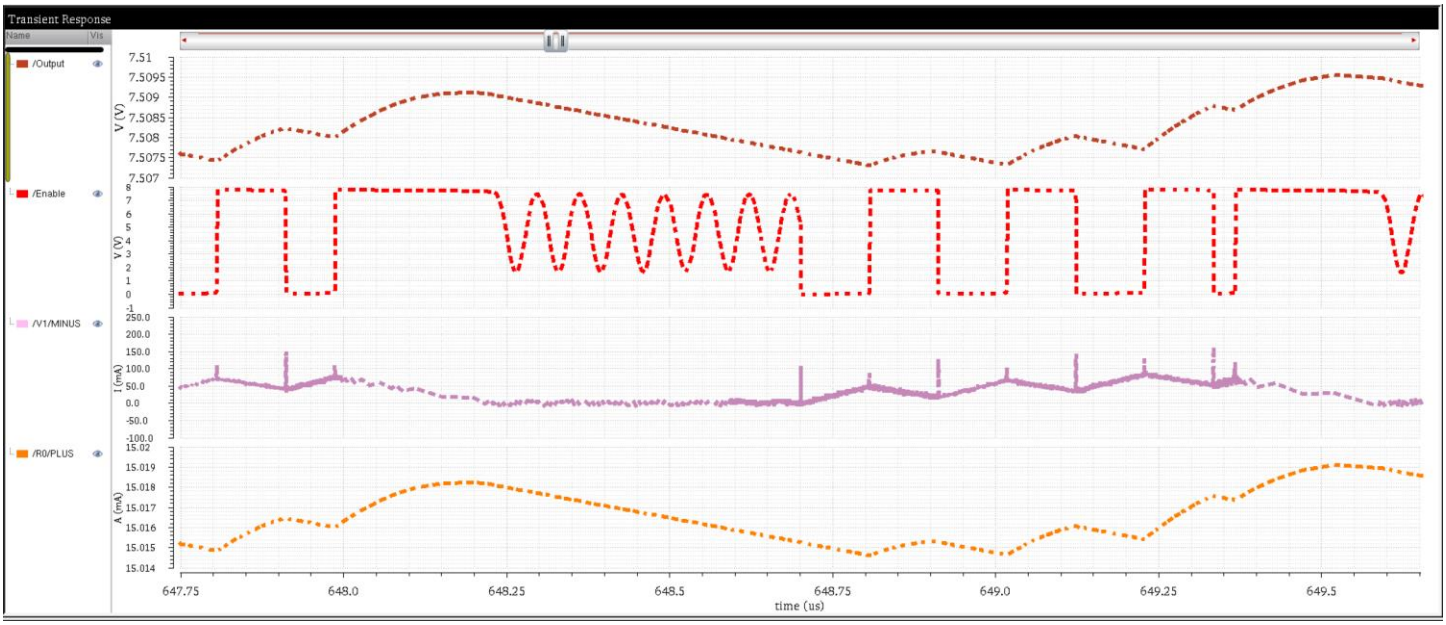
Load and Source Currents at varying temperatures (VDD = 4V)			
Temperature (celsius)	Load Current (mA)	Source Current (A)	efficiency
0	20	0.04068	0.921828909
25	19.99	0.04029	0.930752048
50	19.96	0.04005	0.936329588
75	19.92	0.04004	0.936563437

Load Current Vs. Efficiency Plots:



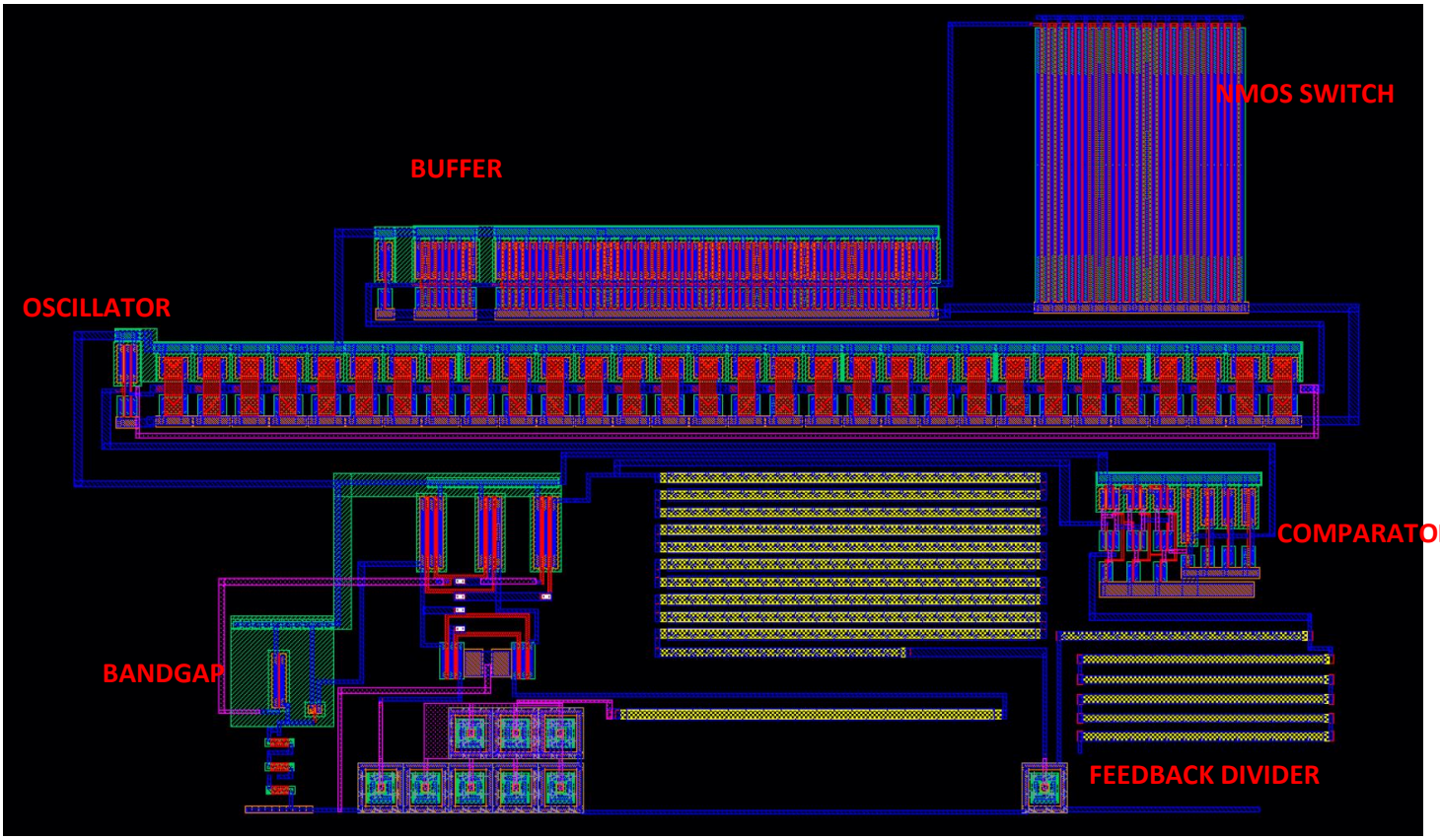


Boost SPS Operation with a Smaller Load Current (15mA) and increased Load Resistor(500):

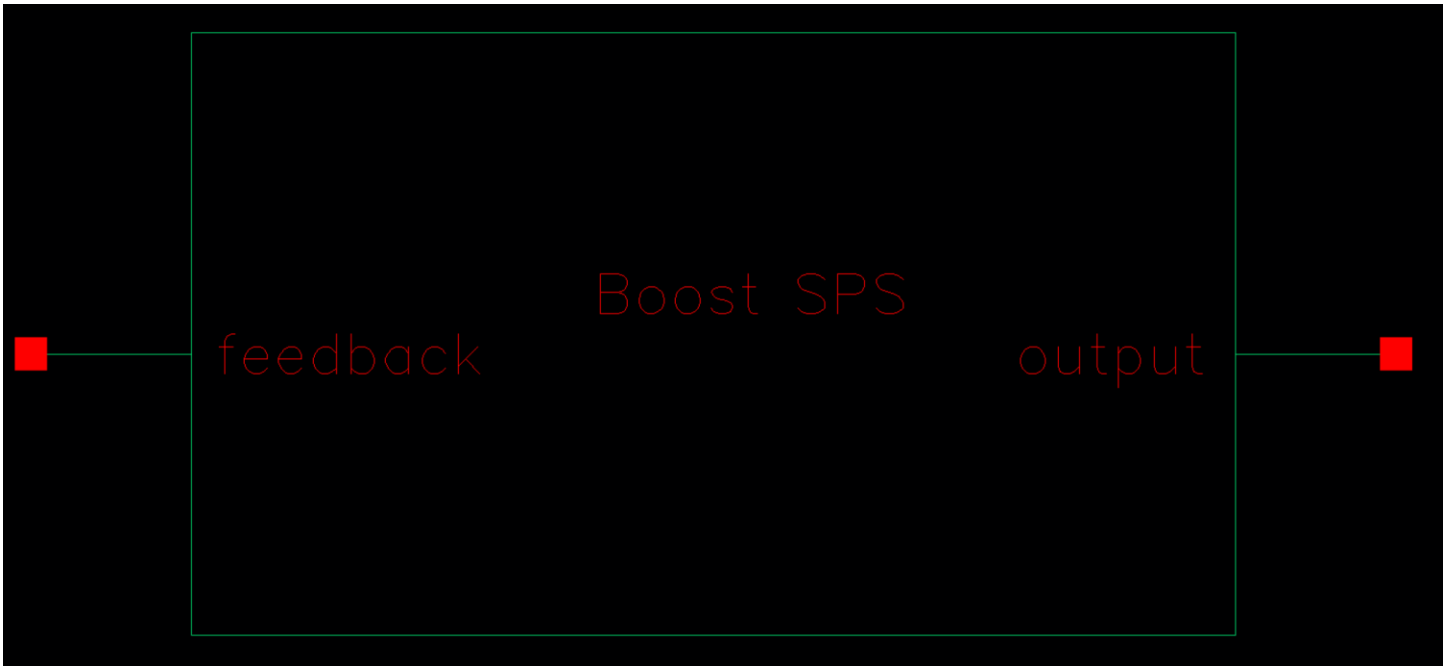


Load and Source Currents at varying temperatures (VDD = 4V)			
VDD	Load Current (mA)	Source Current (A)	efficiency
4.75V	15	0.02644	0.895771956

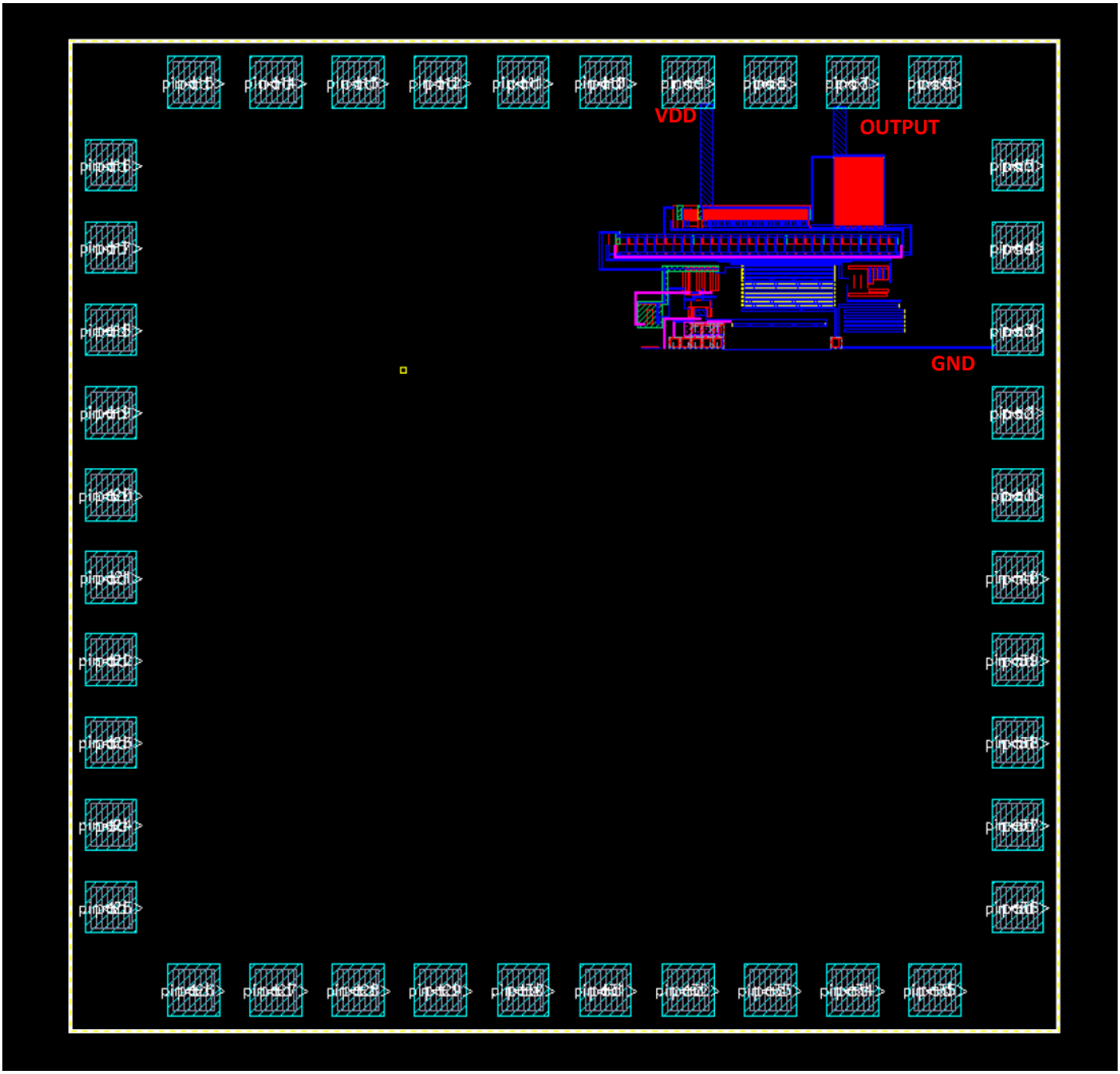
Full layout of the Boost SPS:



Boost SPS Symbol



Boost SPS Layout on Padframe:



Design Considerations:

Comparator:

Choosing the transistor sizes for both the NMOS and PMOS to be equal sizes allowed for a lower power consumption due to these devices being smaller overall. The main disadvantage of this choice may be increased delay through the diff-amp and the switching of the voltage switching point, which needed to be corrected in the buffer stage.

Buffer:

The buffer was chosen to have 3 “beefy” stages to buff up the oscillator signal. It is also standard to use stages that are multiples of 4 of the first stage, but a multiplier of 8 was used for smoother transitions and lower risk of not boosting the signal enough. The drawback to this choice is increased power consumption due to the larger transistor sizes.

Diode:

The Schottky diode was chosen since it was the default diode and it was noted that it was a suboptimal diode. The advantage to using this diode was that it proved the design to be more resilient with the added unnecessary capacitance associated with the model. If models with higher resistance are typically cheaper, then this design choice proves to be a cheaper option if manufactured.

Room for Improvement:

The design for this Boost SPS fulfilled many of the parameters required, namely the load current, source current, and most of the output voltage requirements, however the design did fail when using a VDD of 3.75V. The output voltage failed to reach 7.5V, however increasing VDD to 3.9V brought the output voltage back to 7.5V which is only a small difference from 3.75V. To improve on this, I would explore increasing the off-chip capacitor to hopefully increase the amount of charge that can be supplied to the output in addition to increasing the off-chip inductor. This failure may have been the result of inadequate charging due to these components.

Conclusions:

This design proved to pass the design parameters given minus one test case for the output voltage. The ripple voltage was also kept to a minimum while showing a max ripple of 15mV in most cases with VDD and the Temperature varying. The feedback current also remained between 10uA and 50uA with a load current no greater than 20mA. The design also proved to provide 90% efficiency or greater in every case. Given the performance of this design I believe it would be an acceptable device for real use if it ends up becoming fabricated.